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PTO/SB/05 (8-95)
Approved for use through 9/30/98 OMB 0651-0032
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NEW UTILITY PATENT APPLICATION TRANSMITTAL (to be used for new applications only)	Attorney Docket Number	12 GNC/AUS
	First Named Inventor	Frampton E. ELLIS, III
	Total Pages in this Submission	6

APPLICATION ELEMENTS

Notice: Checklist items mentioned under Application Elements section construct a new utility patent application. Please refer to 37 CFR Sections 506, 601, (37 CFR 1.77, 1.52, 35 USC 111, 112, 113) for a full explanation regarding completeness of an original patent application.

66793 U.S. PTO

05/27/98

- ☒ Fee Transmittal Form (prescribed filing fee(s))
- 2 Specification
- ☒ Title of the Invention
- ☐ Cross References to Related Applications (if applicable)
- ☐ Statement Regarding Federally-sponsored Research/Development (if applicable)
- ☐ Reference to Microfiche Appendix (if applicable)
- ☒ Background of the Invention
- ☒ Brief Summary of the Invention
- ☒ Brief Description of the Drawings (if drawings filed)
- ☒ Detailed Description 80 pages
- ☒ Claim or Claims 8 claims
- ☒ Abstract of the Disclosure
- 3 ☒ Drawing(s) (when necessary as prescribed by 35 USC 113) 17 pages, incl. Figs. 16A-Z & 16AA, 17A-D, 18A-D, 19, & 20A-B
- 4 ☒ Executed Declaration
- 5 Genetic Sequence Submission (if applicable all must be included)
- ☐ Paper Copy
- ☐ Computer Readable Copy
- ☐ Statement Verifying Identical Paper and Computer Readable Copy

ACCOMPANYING APPLICATION PARTS

- 6 ☐ Assignment Papers
- 7 ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
- 8 ☐ Computer Program in Microfiche
- 9 ☐ English Translation Document (if applicable)
- 10 ☐ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations
- 11 ☐ Petition Checklist and Accompanying Petition
- 12 ☐ Preliminary Amendment
- 13 ☐ Proprietary Information
- 14 ☒ Return Receipt Postcard
- 15 ☒ Small Entity Statement
- 16 ☐ Additional Enclosures (please identify below).

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Frampton E. ELLIS, III
Signature	<i>Frampton E. Ellis, III</i>
Date	5/27/98

FOR OFFICIAL USE ONLY

Application Number		Class		Independent Claims	
Date of Receipt	Application Type	GAU		Total Claims	
	Filing Date	Foreign Filing License?		Drawing Sheets	
	Small Entry	Foreign Address?		Special Handling?	

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

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FEE TRANSMITTAL		<i>Complete if Known</i>		
		Application Number		
		Filing Date		
		First Named Inventor	Frampton E. ELLIS, III	
		Group Art Unit		
		Examiner Name		
TOTAL AMOUNT OF PAYMENT	(\$)	395.00	Attorney Docket Number	GNC12US

<p>METHOD OF PAYMENT (check one)</p> <p>1 <input type="checkbox"/> The Commissioner is hereby authorized to charge indicated fees and credit any over payments to</p> <p>Deposit Account Number <input style="width: 150px;" type="text"/></p> <p>Deposit Account Name <input style="width: 150px;" type="text"/></p> <p><input type="checkbox"/> Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17 <input type="checkbox"/> Charge the issue Fee Set in 37 CFR 1.18 at the Making of the Notice of Allowance 37 CFR 1.311(b)</p> <p>2 <input checked="" type="checkbox"/> Payment Enclosed</p> <p style="margin-left: 40px;"><input checked="" type="checkbox"/> Check <input type="checkbox"/> Money Order <input type="checkbox"/> Other</p> <p>FEE CALCULATION (fees effective 10/01/96)</p> <div style="border: 1px solid black; padding: 5px; margin-bottom: 10px;"> <p>1 FILING FEE</p> <table style="width: 100%; font-size: 0.8em;"> <tr> <th>Large Entity</th> <th>Small Entity</th> <th>Fee Code</th> <th>Fee (\$)</th> <th>Fee Code</th> <th>Fee (\$)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> <tr> <td>101</td> <td>201</td> <td>770</td> <td>385</td> <td></td> <td></td> <td>Utility filing fee</td> <td>395</td> </tr> <tr> <td>106</td> <td>206</td> <td>320</td> <td>180</td> <td></td> <td></td> <td>Design filing fee</td> <td></td> </tr> <tr> <td>107</td> <td>207</td> <td>530</td> <td>265</td> <td></td> <td></td> <td>Plant filing fee</td> <td></td> </tr> <tr> <td>108</td> <td>208</td> <td>770</td> <td>385</td> <td></td> <td></td> <td>Reissue filing fee</td> <td></td> </tr> <tr> <td>114</td> <td>214</td> <td>150</td> <td>75</td> <td></td> <td></td> <td>Provisional filing fee</td> <td></td> </tr> <tr> <td colspan="7" style="text-align: right;">SUBTOTAL (1)</td> <td>(\$) 395</td> </tr> </table> </div> <div style="border: 1px solid black; padding: 5px;"> <p>2 CLAIMS</p> <table style="width: 100%; font-size: 0.8em;"> <tr> <th>Total Claims</th> <th>Extra</th> <th>Fee from below</th> <th>Fee Paid</th> </tr> <tr> <td><input style="width: 40px;" type="text"/> - 20 =</td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> </tr> <tr> <td>Independent Claims <input style="width: 40px;" type="text"/> - 3 =</td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> </tr> <tr> <td>Multiple Dependent Claims <input style="width: 40px;" type="text"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> <td><input type="checkbox"/></td> </tr> </table> <table style="width: 100%; font-size: 0.8em; margin-top: 10px;"> <tr> <th>Large Entity</th> <th>Small Entity</th> <th>Fee Code</th> <th>Fee (\$)</th> <th>Fee Code</th> <th>Fee (\$)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> <tr> <td>103</td> <td>203</td> <td>22</td> <td>11</td> <td></td> <td></td> <td>Claims in excess of 20</td> <td></td> </tr> <tr> <td>102</td> <td>202</td> <td>80</td> <td>40</td> <td></td> <td></td> <td>Independent claims in excess of 3</td> <td></td> </tr> <tr> <td>104</td> <td>204</td> <td>260</td> <td>130</td> <td></td> <td></td> <td>Multiple dependent claim</td> <td></td> </tr> <tr> <td>109</td> <td>209</td> <td>80</td> <td>40</td> <td></td> <td></td> <td>Reissue independent claims over original patent</td> <td></td> </tr> <tr> <td>110</td> <td>210</td> <td>22</td> <td>11</td> <td></td> <td></td> <td>Reissue claims in excess of 20 and over original patent</td> <td></td> </tr> <tr> <td colspan="7" style="text-align: right;">SUBTOTAL (2)</td> <td>(\$) <input style="width: 60px;" type="text"/></td> </tr> </table> </div>	Large Entity	Small Entity	Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid	101	201	770	385			Utility filing fee	395	106	206	320	180			Design filing fee		107	207	530	265			Plant filing fee		108	208	770	385			Reissue filing fee		114	214	150	75			Provisional filing fee		SUBTOTAL (1)							(\$) 395	Total Claims	Extra	Fee from below	Fee Paid	<input style="width: 40px;" type="text"/> - 20 =	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Independent Claims <input style="width: 40px;" type="text"/> - 3 =	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Multiple Dependent Claims <input style="width: 40px;" type="text"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Large Entity	Small Entity	Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid	103	203	22	11			Claims in excess of 20		102	202	80	40			Independent claims in excess of 3		104	204	260	130			Multiple dependent claim		109	209	80	40			Reissue independent claims over original patent		110	210	22	11			Reissue claims in excess of 20 and over original patent		SUBTOTAL (2)							(\$) <input style="width: 60px;" type="text"/>	<p>3. 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late filing fee or oath		127	227	50	25			Surcharge - late provisional filing fee or cover sheet		139	139	130	130			Non-English specification		147	147	2,460	2,460			For filing a request for reexamination		112	112	900	900			Requesting publication of SIR prior to Examiner action		113	113	1,790	1,790			Requesting publication of SIR after Examiner action		115	115	215	55			Extension for response within first month		116	216	390	195			Extension for response within second month		117	217	830	465			Extension for response within third month		118	218	1,470	735			Extension for response within fourth month		119	219	300	150			Notice of Appeal		120	220	300	150			Filing a brief in support of an appeal		121	221	260	130			Request for oral hearing		138	138	1,470	1,470			Petition to institute a public use proceeding		140	140	110	55			Petition to revive unavoidably abandoned application		141	241	1,290	645			Petition to revive unintentionally abandoned application		142	242	1,290	645			Utility issue fee (or reissue)		143	243	440	220			Design issue fee		144	244	650	325			Plant issue fee		122	122	130	130			Petitions to the Commissioner		123	123	50	50			Petitions related to provisional applications		126	126	230	230			Submission of Information Disclosure Stmt		581	581	40	40			Recording each patent assignment per property (times number of properties)		146	146	770	385			Filing a submission after final rejection (37 CFR 1.129(a))		149	149	770	385			For each additional invention to be examined (37 CFR 1.129(b))		Other fee (specify) <input style="width: 150px;" type="text"/>								Other fee (specify) <input style="width: 150px;" type="text"/>								SUBTOTAL (3)							(\$) <input style="width: 60px;" type="text"/>
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GLOBAL NETWORK COMPUTERS

BACKGROUND OF THE INVENTION

This invention generally relates to one or more computer networks having computers like personal computers or network computers such as servers with microprocessors preferably linked by broadband transmission means and having hardware, software, firmware, and other means such that at least two parallel processing operations occur that involve at least two sets of computers in the network or in networks connected together, a form of metacomputing. More particularly, this invention relates to one or more large networks composed of smaller networks and large numbers of computers connected, like the Internet, wherein more than one separate parallel or massively parallel processing operation involving more than one different set of computers occurs simultaneously. Even more particularly, this invention relates to one or more such networks wherein more than one (or a very large number of) parallel or massively parallel microprocessing processing operations occur separately or in an interrelated fashion; and wherein ongoing network processing linkages can be established between virtually any microprocessors of separate computers connected to the network.

Still more particularly, this invention relates generally to a network structure or architecture that enables the shared use of network microprocessors for parallel

1 processing, including massive parallel processing, and other
2 shared processing such as multitasking, wherein personal
3 computer owners provide microprocessor processing power to a
4 network, preferably for parallel or massively parallel
5 processing or multitasking, in exchange for network linkage to
6 other personal and other computers supplied by network
7 providers such as Internet Service Providers (ISP's),
8 including linkage to other microprocessors for parallel or
9 other processing such as multitasking. The financial basis of
10 the shared use between owners and providers would be whatever
11 terms to which the parties agree, subject to governing laws,
12 regulations, or rules, including payment from either party to
13 the other based on periodic measurement of net use or
14 provision of processing power or preferably involving no
15 payment, with the network system (software, hardware, etc)
16 providing an essentially equivalent usage of computing
17 resources by both users and providers (since any network
18 computer operated by either entity can potentially be both a
19 user and provider of computing resources alternately (or even
20 simultaneously, assuming multitasking), with potentially an
21 override option by a user (exercised on the basis, for
22 example, of user profile or user's credit line or through
23 relatively instant payment).

24 Finally, this invention relates to a network system
25 architecture including hardware and software that will provide
26 use of the Internet or its future equivalents or successors
27 (and most other networks) without cost to most users of

1 personal computers or most other computers, while also
2 providing those users (and all other users, including of
3 supercomputers) with computer processing performance that will
4 at least double every 18 months through metacomputing means.
5 The metacomputing performance increase provided by this new
6 MetaInternet (or Metanet for short) will be in addition to all
7 other performance increases, such as those already anticipated
8 by Moore's Law.

9 By way of background, the computer industry has been
10 governed over the last 30 years by Moore's Law, which holds
11 that the circuitry of computer chips has been shrunk
12 substantially each year, yielding a new generation of chips
13 every 18 months with twice as many transistors, so that
14 microprocessor computing power is effectively doubled every
15 year and a half.

16 The long term trend in computer chip miniaturization is
17 projected to continue unabated over the next few decades. For
18 example, slightly more than a decade ago a 16 kilobit DRAM
19 memory chip (storing 16,000 data bits) was typical; the
20 current standard 16 megabit chip (16,000,000 data bits),
21 introduced in 1993, is a thousand times larger. Industry
22 projections are for 16 gigabit memory chips (16,000,000,000
23 data bits) to be introduced in 2008 and 64 gigabit chips in
24 2011, with 16 terabit chips (16,000,000,000,000 data bits)
25 conceivable by the mid-to-late 2020's. This is a thousand-
26 fold increase regularly every fifteen years. Hard drive speed
27 and capacity are also growing at a spectacular rate, even

1 higher than that of semiconductor microchips in recent years.

2 Similarly regular and enormous improvements are
3 anticipated to continue in microprocessor computing speeds,
4 whether measured in simple clock speed or MIPS (millions of
5 instructions for second) or numbers of transistors per chip.
6 For example, performance has improved by four or five times
7 every three years since Intel launched its X86 family of
8 microprocessors used in the currently dominant "Wintel"
9 standard personal computers. The initial Intel Pentium Pro
10 microprocessor was introduced in 1995 and is a thousand times
11 faster than the first IBM standard PC microprocessor, the
12 Intel 8088, which was introduced in 1979. The fastest of
13 current microprocessors like Digital Equipment Corp.'s Alpha
14 chip is faster than the processor in the original Cray Y-MP
15 supercomputer.

16 Both microprocessors and software (and firmware and
17 other components) are also evolving from 8 bit and 16 bit
18 systems into 32 bit systems that are becoming the standard
19 today, with some 64 bit systems like the DEC Alpha already
20 introduced and more coming, such as Intel's Merced
21 microprocessor in 1999, with future increases to 128 bit
22 likely some later.

23 A second major development trend in the past decade or
24 so has been the rise of parallel processing, a computer
25 architecture utilizing more than one CPU microprocessor (often
26 many more, even thousands of relatively simple
27 microprocessors, for massively parallel processing) linked

1 together into a single computer with new operating systems
2 having modifications that allow such an approach. The field
3 of supercomputing has been taken over by this approach,
4 including designs utilizing many identical standard personal
5 computer microprocessors.

6 Hardware, firmware, software and other components
7 specific to parallel processing are in a relatively early
8 stage of development compared to that for single processor
9 computing, and therefore much further design and development
10 is expected in the future to better maximize the computing
11 capacity made possible by parallel processing. One potential
12 benefit that will likely be available soon is system
13 architecture that does not rely on the multiple
14 microprocessors having to share memory, thereby allowing more
15 independent operation of those microprocessors, each with
16 their own discrete memory, like current personal computers,
17 workstations and most other computer systems architecture; for
18 unconstrained operation, each individual microprocessor must
19 have rapid access to sufficient memory.

20 Several models of personal computers are now available
21 with more than one microprocessor. It seems inevitable that
22 in the future personal computers, broadly defined to include
23 versions not currently in use, will also employ parallel
24 computing utilizing multiple microprocessors or massively
25 parallel computing with very large numbers of microprocessors.

26 Future designs, such Intel's Merced chip, will have a
27 significant number of parallel processors on a single

1 microprocessor chip.

2 A form of parallel processing called superscalar
3 processing is also being employed within microprocessor design
4 itself. The current generation of microprocessors such as the
5 Intel Pentium have more than one data path within the
6 microprocessor in which data can be processed, with two to
7 three paths being typical now and as many as eight in 1998 in
8 IBM's new Power 3 microprocessor chip.

9 The third major development trend is the increasing size
10 of bandwidth, which is a measure of communications power or
11 transmission speed (in terms of units of data per second)
12 between computers connected by a network. Before now, the
13 local area networks and telephone lines typically linking
14 computers including personal computers have operated at speeds
15 much lower than the processing speeds of a personal computer.
16 For example, a typical 1997 Intel Pentium operates at 100
17 MIPS (millions of instructions per second), whereas the most
18 common current Ethernet connecting PC's is roughly 10 times
19 slower at 10 megabits per second (Mbps), although some
20 Ethernet connections are now 100 Mbps) and telephone lines are
21 very much slower, the highest typical speed in 1998 being
22 about 56 kilobits (reached only during downloads, however).

23 Now, however, the situation is expected to change
24 dramatically, with bandwidth or transmission speed being
25 anticipated to expand from 5 to 100 times as fast as the rise
26 of microprocessor speeds, due to the use of coaxial cable,
27 wireless, and especially fiber optic cable, instead of old

1 telephone twisted pair lines. Telecommunication providers are
2 now making available fiber connections supporting bandwidth of
3 40 gigabits and higher.

4 Technical improvements are expected in the near term
5 which will make it possible to carry over 2 gigahertz
6 (billions of cycles per second) on each of 700 wavelength
7 streams, adding up to more than 1,400 gigahertz on every
8 single fiber thread. Experts currently estimate that the
9 bandwidth of optical fiber has been utilized one million times
10 less fully than the bandwidth of coaxial or twisted pair
11 copper lines. Within a decade, 10,000 wavelength streams per
12 fiber are expected and 20-80 wavelengths on a single fiber is
13 already commercially available.

14 Other network connection developments such as
15 asynchronous transfer mode (ATM) and digital signal
16 processors, which are improving their price/performance
17 tenfold every two years, are also supporting the rapid
18 increase in bandwidth. The increase in bandwidth reduces the
19 need for switching and switching speed will be greatly
20 enhanced when practical optical switches are introduced in the
21 fairly near future, potentially reducing costs substantially.

22 The result of this huge bandwidth increase will be
23 extraordinary: within just a few years it will be technically
24 possible to connect virtually any computer to a network at a
25 speed that equals or exceeds the computer's own internal
26 system bus speed, even as that bus speed itself is increasing
27 significantly. The system bus of a computer is its internal

1 network connecting many or most of its internal components
2 such as microprocessor, random access memory (RAM), hard-
3 drive, modem, floppy drive, and CD-ROM; for recent personal
4 computers it has been only about 40 megabits per second, but
5 is up to 133 megabits per second on Intel's Pentium PCI bus in
6 1995. IBM's 1998 Power3 microprocessor chip has a system bus
7 of 1.6 gigabits per second.

8 Despite these tremendous improvements anticipated in the
9 future, the unfortunate present reality is that a typical
10 personal computer (PC) is already so fast that its
11 microprocessor is essentially idle during most of the time the
12 PC is in actual use and that operating time itself is but a
13 small fraction of those days the PC is even in any use at all.

14 The reality is that nearly all PC's are essentially idle
15 during roughly all of their useful life. A realistic estimate
16 is that its microprocessor is in an idle state 99.9% of the
17 time (disregarding current unnecessary microprocessor busywork
18 like executing screen saver programs, which have been made
19 essentially obsolete by power-saving CRT monitor technology,
20 which is now standard in the PC industry).

21 Given the fact that the reliability of PC's is so
22 exceptionally high now, with the mean time to failure of all
23 components typically several hundred thousand hours or more,
24 the huge idle time of PC's represents a total loss; given the
25 high capital and operating costs of PC's, the economic loss is
26 very high. PC idle time does not in effect store a PC, saving
27 it for future use, since the principle limiting factor to

1 continued use of today's PC's is obsolescence, not equipment
2 failure from use.

3 Moreover, there is growing concern that Moore's Law,
4 which as noted above holds that the constant miniaturization
5 of circuits results in a doubling of computing power every 18
6 months, cannot continue to hold true much longer. Indeed,
7 Moore's Law may now be nearing its limits for silicon-based
8 devices, perhaps by as early as 2004, and no new technologies
9 have yet emerged that currently seem with reasonable certainty
10 to have the potential for development to a practical level by
11 then, although many recent advances have the potential to
12 maintain Moore's Law.

13 SUMMARY OF THE INVENTION

14 However, the confluence of all three of the established
15 major trends summarized above -- supercomputer-like personal
16 computers, the spread of parallel processing using personal
17 computer microprocessors (particularly massively parallel
18 processing), and the enormous increase in network
19 communications bandwidth -- will make possible in the near
20 future a surprising solution to the hugely excessive idleness
21 problem of personal computers (and to the problematic possible
22 end of Moore's Law), with very high potential economic
23 savings.

24 The solution is use those mostly idle PC's (or their
25 equivalents or successors) to build a parallel or massively
26 parallel processing computer utilizing a very large network
27 like the Internet or, more specifically, like the World Wide

1 Web (WWW), or their equivalents or eventual successors like
2 the MetaInternet (and including Internet II, which is under
3 development now and which will utilize much broader bandwidth
4 and will coexist with the Internet, the structure of which is
5 in ever constant hardware and software upgrade and including
6 the SuperInternet based on essentially all optical fiber
7 transmission) with extremely broad bandwidth connections and
8 virtually unlimited data transmission speed.

9 The prime characteristic of the Internet is of course
10 the very large number of computers of all sorts already linked
11 to it, with the future potential for effectively universal
12 connection; it is a network of networks of computers that
13 provides nearly unrestricted access (other than cost)
14 worldwide. The soon-to-be available very broad bandwidth of
15 network communications can be used to link personal computers
16 externally in a manner at least equivalent to the faster
17 internal system buses of the personal computers, so that no
18 external processing constraint will be imposed on linked
19 personal computers by data input or output, or throughput; the
20 speed of the microprocessor itself will be the only processing
21 constraint of the system, other than the internal system bus
22 design.

23 This will make external parallel processing possible,
24 including massively parallel processing, in a manner
25 paralleling more conventional internal parallel processing,
26 call superscalar processing.

27 The World Wide Web (or its equivalents or successors)

1 would thereby have the potential to be transformed into a huge
2 virtual massively parallel processing computer or computers,
3 with a unique potential through its established hyperlinks
4 connections to operate in a manner at least somewhat like a
5 human neural network or neural networks, since the speed of
6 transmission in the linkages would be so great that any
7 linkage between two microprocessors would be virtually
8 equivalent to direct, physically close connections between
9 those microprocessors.

10 With further development, digital signal processor-type
11 microprocessors and/or analogue microprocessors may be
12 particularly advantageous for this approach, either alone or
13 in conjunction with conventional microprocessors and/or those
14 new microprocessors described in this application. Networks
15 with WWW-type hyperlinks incorporating digital signal
16 processor-type microprocessor (or successors or equivalents)
17 could operate separately from networks of conventional
18 microprocessors (or successors or equivalents) or with one or
19 more connections between such differing networks or with
20 relatively complete integration between such differing
21 networks. Simultaneous operation across the same network
22 connection structure should be possible, employing non-
23 interfering transmission links.

24 Such extremely broad bandwidth networks of computers
25 will enable every PC to be fully utilized or nearly so.
26 Because of the extraordinary extent to which existing PC's are
27 currently idle, at optimal performance this new system will

1 potentially result in a thousand-fold increase in computer
2 power available to each and every PC user (and any other
3 user); and, on demand, almost any desired level of increased
4 power, limited mostly by the increased cost, which however
5 would be relatively far less than possible from any other
6 conceivable computer network configuration. This
7 revolutionary increase is on top of the extremely rapid, but
8 evolutionary increases already occurring in the
9 computer/network industry discussed above.

10 The metacomputing hardware and software means of the
11 MetaInternet will provide performance increases that will
12 likely at least double every eighteen months based on the
13 doubling of personal computers shared in a typical parallel
14 processing operation by a standard PC user, starting first
15 with at least 2 PC's, then about 4, about 8, about 16, about
16 32, about 64, about 128, about 256, and about 512. After
17 about fifteen years, each standard PC user will likely be able
18 to use about 1024 personal computers for parallel processing
19 or any other shared computing use, while generally using the
20 Internet or its successors like the MetaInternet for free. At
21 the other end of the performance spectrum, supercomputers will
22 experience a similar performance increase generally, but
23 ultimately the performance increase is limited primarily by
24 cost of adding temporary network linkages to available PC's,
25 so there is definite potential for a quantum leap in
26 supercomputer performance.

27 Network computer systems as described above offer almost

1 limitless flexibility due to the abundant supply of heretofore
2 idle connected microprocessors. This advantage would allow
3 "tightly coupled" computing problems (which normally are
4 difficult to process in parallel) to be solved without knowing
5 in advance (as is now necessary in relatively massively
6 parallel processing) how many processors are available, what
7 they are and their connection characteristics. A minimum
8 number of equivalent processors (with equivalent other specs)
9 can be easily found nearby in a massive network like the
10 Internet and assigned within the network from those multitudes
11 available nearby. Moreover, the number of microprocessors
12 used can be almost completely flexible, depending on the
13 complexity of the problem, and limited only by cost. The
14 current problem of time delay will be solved largely by the
15 widespread introduction of extremely broad bandwidth
16 connections between computers processing in parallel.

17 BRIEF DESCRIPTION OF THE DRAWINGS

18 Figure 1 is a simplified diagram of a section of a
19 computer network, such as the Internet, showing an embodiment
20 of a meter means which measures flow of computing during a
21 shared operation such as parallel processing between a typical
22 PC user and a network provider.

23 Figure 2 is a simplified diagram of a section of a
24 computer network, such as the Internet, showing an embodiment
25 of another meter means which measures the flow of network
26 resources, including shared processing, being provided to a
27 typical PC user and a network provider.

1 Figure 3 is a simplified diagram of a section of a
2 computer network, such as the Internet, showing an embodiment
3 of another meter means which, prior to execution, estimates
4 the level of network resources, and their cost, of a shared
5 processing operation requested by a typical PC user from a
6 network provider.

7 Figure 4A-4C are simplified diagrams of a section of a
8 computer network, such as the Internet, showing in a sequence
9 of steps an embodiment of a selection means whereby a shared
10 processing request by a PC is matched with a standard preset
11 number of other PC's to execute shared operation.

12 Figure 5 is a simplified diagram of a section of a
13 computer network, such as the Internet, showing an embodiment
14 of a control means whereby the PC, when idled by its user, is
15 made available to the network for shared processing
16 operations.

17 Figure 6 is a simplified diagram of a section of a
18 computer network, such as the Internet, showing an embodiment
19 of a signal means whereby the PC, when idled by its user,
20 signals its availability to the network for shared processing
21 operations.

22 Figure 7 is a simplified diagram of a section of a
23 computer network, such as the Internet, showing an embodiment
24 of a receiver and/or interrogator means whereby the network
25 receives and/or queries the availability for shared processing
26 status of a PC within the network.

27 Figure 8 is a simplified diagram of a section of a

1 computer network, such as the Internet, showing an embodiment
2 of a selection and/or utilization means whereby the network
3 locates available PC's in the network that are located closest
4 to each other for shared processing.

5 Figure 9 is a simplified diagram of a section of a
6 computer network, such as the Internet, showing an embodiment
7 of a system architecture for conducting a request imitated by
8 a PC for a search using parallel processing means that
9 utilizes a number of networked PC's.

10 Figures 10A-10I are simplified diagrams of a section of
11 a computer network, such as the Internet, showing an
12 embodiment of a system architecture utilizing a firewall to
13 separate that part of a networked PC (including a system
14 reduced in size to a microchip) that is accessible to the
15 network for shared processing from a part that is kept
16 accessible only to the PC user; also showing the alternating
17 role that preferably each PC in the network can play as either
18 a master or slave in a shared processing operation involving
19 one or more slave PC's in the network; showing a home or
20 business network system; in addition, showing PC and PC
21 microchips controlled by a controller (including remote) with
22 limited or no processing capability; and showing PC and PC
23 microchips in which a firewall 50 is can be reconfigured by a
24 PC user.

25 Figure 11 is a simplified diagram of a section of a
26 computer network, such as the Internet, showing an embodiment
27 of a system architecture for connecting clusters of PC's to

1 each other by wireless means, to create the closest possible
2 (and therefore fastest) connections.

3 Figure 12 is a simplified diagram of a section of a
4 computer network, such as the Internet, showing an embodiment
5 of a system architecture for connecting PC's to a satellite by
6 wireless means.

7 Figure 13 is a simplified diagram of a section of a
8 computer network, such as the Internet, showing an embodiment
9 of a system architecture providing a cluster of networked PC's
10 with complete interconnectivity by wireless means.

11 Figure 14A is a simplified diagram of a section of a
12 computer network, such as the Internet, showing an embodiment
13 of a transponder means whereby a PC can identify one or more
14 of the closest available PC's in a network cluster to
15 designate for shared processing by wireless means. Figure 14B
16 shows clusters connected wirelessly; Figure 14C shows a
17 wireless cluster with transponders and with a network wired
18 connection to Internet; Figure 14D shows a network
19 client/server wired system with transponders.

20 Figure 15 is a simplified diagram of a section of a
21 computer network, such as the Internet, showing an embodiment
22 of a routing means whereby a PC request for shared processing
23 can be routed within a network using preferably broad
24 bandwidth connection means to another area in a network with
25 one or more idle PC's available.

26 Figures 16A-16Z and 16AA show a new hierarchical network
27 architecture for personal computers and/or microprocessors

1 based on subdivision of parallel processing or multi-tasking
2 operations through a number of levels down to a processing
3 level.

4 Figures 17A-17D show a firewall 50 with a dual function,
5 including that of protecting Internet users (and/or other
6 network users sharing use) of one or more slave personal
7 computers PC 1 or microprocessors 40 from unauthorized
8 surveillance or intervention by an owner/operator of those
9 slave processors.

10 Figures 18A-18D show designs for one or more virtual
11 quantum computers integrated into one or more digital
12 computers.

13 Figure 19 shows special adaptations to allow the use of
14 idle automobile computers to be powered and connected to the
15 Internet (or other net) for parallel or multi-tasking
16 processing.

17 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

18 The new network computer will utilize PC's as providers
19 of computing power to the network, not just users of network
20 services. These connections between network and personal
21 computer are enabled by a new form of computer/network
22 financial structure that is rooted on the fact that economic
23 resources being provided the network by PC owners (or leaser)
24 are similar in value to those being provided by the network
25 provider providing connectivity.

26 Unlike existing one way functional relationships between
27 network providers such as internet service providers (often

1 currently utilizing telecommunications networks for
2 connectivity) and PC users, wherein the network provider
3 provides access to a network like the Internet for a fee (much
4 like cable TV services), this new relationship would recognize
5 that the PC user is also providing the network access to the
6 user's PC for parallel computing use, which has a similar
7 value. The PC thus both provides and uses services on the
8 network, alternatively or potentially even virtually
9 simultaneously in a multitasking mode.

10 This new network would operate with a structural
11 relationship that would be roughly like that which presently
12 can exist between an electrical power utility and a small
13 independent power generator connected to the utility, wherein
14 electrical power can flow in either between utility and
15 independent direction depending on the operating decisions of
16 both parties and at any particular point in time each party is
17 in either a debt or credit position relative to the other
18 based on the net direction of that flow for a given period,
19 and is billed accordingly. In the increasingly deregulated
20 electrical power industry, electrical power (both its creation
21 and transmission) is becoming a commodity bought and sold in a
22 competitive marketplace that crosses traditional borders.
23 With the structural relationship proposed here for the new
24 network, parallel free market structures should develop over
25 time in a new computer power industry dominated by networks of
26 personal computers in all their current and future forms
27 providing shared processing.

1 For this new network and its structural relationships, a
2 network provider is defined in the broadest possible way as
3 any entity (corporation or other business, government, not-
4 for-profit, cooperative, consortium, committee, association,
5 community, or other organization or individual) that provides
6 personal computer users (very broadly defined below) with
7 initial and continuing connection hardware and/or software
8 and/or firmware and/or other components and/or services to any
9 network, such as the Internet and Internet II or WWW or their
10 present or future equivalents, coexistors or successors, like
11 the herein proposed MetaInternet, including any of the current
12 types of Internet access providers (ISP's) including
13 telecommunication companies, television cable or broadcast
14 companies, electrical power companies, satellite
15 communications companies, or their present or future
16 equivalents, coexistors or successors. The connection means
17 used in the networks of the network providers, including
18 between personal computers or equivalents or successors, would
19 preferably be very broad bandwidth, by such means as fiber
20 optic cable or wireless for example, but not excluding any
21 other means, including television coaxial cable and telephone
22 twisted pair, as well as associated gateways, bridges,
23 routers, and switches with all associated hardware and/or
24 software and/or firmware and/or other components and their
25 present or future equivalents or successors. The computers
26 used by the providers include any computers, including
27 mainframes, minicomputers, servers, and personal computers,

1 and associated their associated hardware and/or software
2 and/or firmware and/or other components, and their present or
3 future equivalents or successors.

4 Other levels of network control beyond the network
5 provider will also exist to control any aspect of the network
6 structure and function, any one of which levels may or may not
7 control and interact directly with the PC user. For example,
8 at least one level of network control like the World Wide Web
9 Consortium (W3C) or Internet Society (ISOC) or other ad hoc
10 industry consortia) would establish and ensure compliance with
11 any prescribed network standards and/or protocols and/or
12 industry standard agreements for any hardware and/or software
13 and/or firmware and/or other component connected to the
14 network. Under the consensus control of these
15 consortia/societies, other levels of network control would
16 deal with administration and operation of the network. These
17 other levels of network control might be constituted by any
18 network entity, including those defined immediately above for
19 network providers.

20 The principal defining characteristic of the network
21 provided being communication connections (including hardware
22 and/or software and/or firmware and/or other component) of any
23 form, including electromagnetic (such as light and radio or
24 microwaves) and electrochemical (and not excluding biochemical
25 or biological), between PC users, with connection (either
26 directly or indirectly) to the largest number of users
27 possible being highly advantageous, such as networks like the

1 Internet (and Internet II and SuperInternet) and WWW and
2 equivalents and successors, like the MetaInternet. Multiple
3 levels of such networks will likely coexist with different
4 technical capabilities, like Internet and Internet II, but
5 would have interconnection and therefore would communicate
6 freely between levels, for such standard network functions as
7 electronic mail.

8 And a personal computer (PC) user is defined in the
9 broadest possible way as any individual or other entity using
10 a personal computer, which is defined as any computer, digital
11 or analog or neural, particularly including microprocessor-
12 based personal computers having one or more microprocessors
13 (each including one or more parallel processors) in their
14 general current form (hardware and/or software and/or firmware
15 and/or any other component) and their present and future
16 equivalents or successors, such as workstations, network
17 computers, handheld personal digital assistants, personal
18 communicators such as telephones and pagers, wearable
19 computers, digital signal processors, neural-based computers
20 (including PC's), entertainment devices such as televisions,
21 video tape recorders, videocams, compact or digital video disk
22 (CD or DVD) player/recorders, radios and cameras, other
23 household electronic devices, business electronic devices such
24 as printers, copiers, fax machines, automobile or other
25 transportation equipment devices, and other current or
26 successor devices incorporating one or more microprocessors
27 (or functional or structural equivalents), especially those

1 used directly by individuals, utilizing one or more
2 microprocessors, made of inorganic compounds such as silicon
3 and/or other inorganic or organic compounds; current and
4 future forms of mainframe computers, minicomputers,
5 microcomputers, and even supercomputers are also be included.

6 Such personal computers as defined above have owners or
7 leasers, which may or may not be the same as the computer
8 users. Continuous connection of computers to the network,
9 such as the Internet, WWW, or equivalents or successors, is
10 preferred.

11 Parallel processing is defined as one form of shared
12 processing as involving two or more microprocessors involved
13 in solving the same computational problem or other task.

14 Massively parallel microprocessor processing involves large
15 numbers of microprocessors. In today's technology, massive
16 parallel processing can probably be considered to be about 64
17 microprocessors (referred to in this context as nodes) and
18 over 7,000 nodes have been successfully tested in an Intel
19 supercomputer design using PC microprocessors (Pentium Pros).

20 It is anticipated that continued software improvements will
21 make possible a much larger number of nodes, very possibly
22 limited only by the number of microprocessors available for
23 use on a given network, even an extraordinarily large one like
24 the Internet or its equivalents and/or successors, like the
25 MetaInternet.

26 Broadband wavelength or broad bandwidth network
27 transmission is defined here to mean a transmission speed

1 (usually measured in bits per second) that is at least high
2 enough (or roughly at least equivalent to the internal clock
3 speed of the microprocessor or microprocessors times the
4 number of microprocessor channels equaling instructions per
5 second or operations per second or calculations per second) so
6 that the processing input and output of the microprocessor is
7 substantially unrestricted, particularly including at peak
8 processing levels, by the bandwidth of the network connections
9 between microprocessors that are performing some form of
10 parallel processing, particularly including massive parallel
11 processing. Since this definition is dependent on
12 microprocessor speed, it will increase as microprocessor
13 speeds increase. A rough example might be a current 100 MIPS
14 (millions instructions per second) microprocessor, for which a
15 broad bandwidth connection would be greater than 100 megabits
16 per second (Mbps); this is a very rough approximation.
17 However, a preferred connection means referenced above is
18 fiber optic cable, which currently already provides multiple
19 gigabit bandwidth on single fiber thread and will improve
20 significantly in the future, so the preferred general use of
21 fiber optic cable virtually assures broad bandwidth for data
22 transmission that is far greater than microprocessor speed to
23 provide data to be transmitted. The connection means to
24 provide broad bandwidth transmission can be either wired or
25 wireless, with wireless generally preferred for mobile
26 personal computers (or equivalents or successors) and as
27 otherwise indicated below. Wireless connection bandwidth is

1 also increasing rapidly and can be considered to offer
2 essentially the same principal benefit as fiber optic cable:
3 external data transmission speed in a network that far exceeds
4 internal data processing speed in any computer.

5 The financial basis of the shared use between owners/
6 leasers and providers would be whatever terms to which the
7 parties agree, subject to governing laws, regulations, or
8 rules, including payment from either party to the other based
9 on periodic measurement of net use or provision of processing
10 power.

11 In one embodiment, as shown in Figure 1, in order for
12 this network structure to function effectively, there would be
13 a meter device 5 (comprised of hardware and/or software and/or
14 firmware and/or other component) to measure the flow of
15 computing power between PC 1 user and network 2 provider,
16 which might provide connection to the Internet and/or World
17 Wide Web and/or Internet II and/or any present or future
18 equivalent or successor 3, like the MetaInternet. In one
19 embodiment, the PC user should be measured by some net rating
20 of the processing power being made available to the network,
21 such as net score on one or more standard tests measuring
22 speed or other performance characteristics of the overall
23 system speed, such as PC Magazine's benchmark test program, ZD
24 Winstone (potentially including hardware and/or software
25 and/or firmware and/or other component testing) or specific
26 individual scores for particularly important components like
27 the microprocessor (such as MIPS or millions of instructions

1 per second) that may be of application-specific importance,
2 and by the elapsed time such resources were used by the
3 network. In the simplest case, for example, such a meter need
4 measure only the time the PC was made available to the network
5 for processing 4, which can be used to compare with time the
6 PC used the network (which is already normally measured by the
7 provider, as discussed below) to arrive at a net cost;
8 potential locations of such a meter include at a network
9 computer such as a server, at the PC, and at some point on the
10 connection between the two. Throughput of data in any
11 standard terms is another potential measure.

12 In another embodiment, as shown in Figure 2, there also
13 would be a meter device 7 (comprised of hardware and/or
14 software and/or firmware and/or other component) that measures
15 the amount of network resources 6 that are being used by each
16 individual PC 1 user and their associated cost. This would
17 include, for example, time spent doing conventional
18 downloading of data from sites in the network or broadcast
19 from the network 6. Such metering devices currently exist to
20 support billing by the hour of service or type of service is
21 common in the public industry, by providers such as America
22 Online, Compuserve, and Prodigy. The capability of such
23 existing devices would be enhanced to include a measure of
24 parallel processing resources that are allocated by the
25 Internet Service Provider or equivalent to an individual PC
26 user from other PC users 6, also measuring simply in time.
27 The net difference in time 4 between the results of meter 5

1 and meter 7 for a given period would provide a reasonable
2 billing basis.

3 Alternately, as shown in Figure 3, a meter 10 would also
4 estimate to the individual PC user prospectively the amount of
5 network resources needed to fulfill a processing request from
6 the PC user to the network (provider or other level of network
7 control) and associated projected cost, provide a means of
8 approving the estimate by executing the request, and a
9 realtime readout of the cost as it occurs (alternatively, this
10 meter might be done only to alert 9 the PC user that a given
11 processing request 8 falls outside normal, previously accepted
12 parameters, such as level of cost). To take the example of an
13 unusually deep search request, a priority or time limit and
14 depth of search can be highly useful criteria or limiting
15 parameters that the user can determine or set with the device.

16 Preferably, the network would involve no payment between
17 users and providers, with the network system (software,
18 hardware, etc) providing an essentially equivalent usage of
19 computing resources by both users and providers (since any
20 network computer operated by either entity can potentially be
21 both a user and provider of computing resources (even
22 simultaneously, assuming multitasking), with potentially an
23 override option by a user (exercised on the basis, for
24 example, of user profile or user's credit line or through
25 relatively instant payment).

26 Preferably, as shown in Figure 4, the priority and
27 extent of use of PC and other users can be controlled on a

1 default-to-standard-of-class-usage basis by the network
2 (provider or other) and overridden by the user decision on a
3 basis prescribed by the specific network provider (or by
4 another level of network control). One simple default basis
5 would be to expend up to a PC's or other user's total credit
6 balance with the provider described above and the network
7 provider then to provide further prescribed service on an debt
8 basis up to some set limit for the user; different users might
9 have different limits based on resources and/or credit
10 history.

11 A specific category of PC user based, for example, on
12 specific microprocessor hardware owned or leased, might have
13 access to a set maximum number of parallel PC's or
14 microprocessors, with smaller or basic users generally having
15 less access and vice versa. Specific categories of users
16 might also have different priorities for the execution of
17 their processing by the network. A very wide range of
18 specific structural forms between user and provider are
19 possible, both conventional and new, based on unique features
20 of the new network computer system of shared processing
21 resources.

22 For example, in the simplest case, in an initial system
23 embodiment, as shown in Fig. 4A, a standard PC 1 user request
24 11 for a use involving parallel processing might be defaulted
25 by system software 13, as shown in Fig. 4B, to the use of only
26 one other essentially identical PC 1₂ microprocessor for
27 parallel processing or multitasking, as shown in Figure 4C;

1 larger standard numbers of PC microprocessors, such as about
2 three PC's at the next level, as shown in later Figure 10G
3 (which could also illustrate a PC 1 user exercising an
4 override option to use a level of services above the default
5 standard of one PC microprocessor, presumably at extra cost),
6 for a total of about four, then about 8, about 16, about 32,
7 about 64 and so on, or virtually any number in between, would
8 be made available as the network system is upgraded over time,
9 as well as the addition of sophisticated override options.
10 Eventually many more PC microprocessors would be made
11 available to the standard PC user (virtually any number),
12 preferably starting at about 128, then about 256, then about
13 512, then about 1024 and so on over time, as the network and
14 all of its components are gradually upgraded to handle the
15 increasing numbers. System scalability at even the standard
16 user level is essentially unlimited over time.

17 Preferably, for most standard PC users (including
18 present and future equivalents and successors), connection to
19 the Internet (or present or future equivalents or successors
20 like the MetaInternet) would be at no cost to PC users, since
21 in exchange for such Internet access the PC users would
22 generally make their PC, when idle, available to the network
23 for shared processing. Preferably, then, competition between
24 Internet Service Providers (including present and future
25 equivalents and successors) for PC user customers would be
26 over such factors as the convenience and quality of the access
27 service provided and of shared processing provided at no

1 addition cost to standard PC users, or on such factors as the
2 level of shared processing in terms, for example of number of
3 slave PC's assigned on a standard basis to a master PC. The
4 ISP's would also compete for parallel processing operations,
5 from inside or outside the ISP Networks, to conduct over their
6 networks.

7 In addition, as shown in Figure 5, in another embodiment
8 there would be a (hardware and/or software and/or firmware
9 and/or other) controlling device to control access to the
10 user's PC by the network. In its simplest form, such as a
11 manually activated electromechanical switch, the PC user could
12 set this controller device to make the PC available to the
13 network when not in use by the PC user. Alternatively, the
14 PC user could set the controller device to make the PC
15 available to the network whenever in an idle state, however
16 momentary, by making use of multitasking hardware and/or
17 software and/or firmware and/or other component (broadcast or
18 "push" applications from the Internet or other network could
19 still run in the desktop background).

20 Or, more simply, as shown in Figure 5A, whenever the
21 state that all user applications are closed and the PC 1 is
22 available to the network 14 (perhaps after a time delay set by
23 the user, like that conventionally used on screensaver
24 software) is detected by a software controller device 12
25 installed in the PC, the device 12 would signal 15 the network
26 computer such as a server 2 that the PC available to the
27 network, which could then control the PC 1 for parallel

1 processing or multitasking by another PC. Such shared
2 processing can continue until the device 12 detects the an
3 application being opened 16 in the first PC (or at first use
4 of keyboard, for quicker response, in a multitasking
5 environment), when the device 12 would signal 17 the network
6 computer such as a server 2 that the PC is no longer available
7 to the network, as shown in Figure 5B, so the network would
8 then terminate its use of the first PC.

9 In a preferred embodiment, as shown in Figure 6, there
10 would be a (hardware and/or software and/or firmware and/or
11 other component) signaling device 18 for the PC 1 to indicate
12 or signal 15 to the network the user PC's availability 14 for
13 network use (and whether full use or multitasking only) as
14 well as its specific (hardware/software/firmware/other
15 components) configuration 20 (from a status 19 provided by the
16 PC) in sufficient detail for the network or network computer
17 such as a server 2 to utilize its capability effectively. In
18 one embodiment, the transponder device would be resident in
19 the user PC and broadcast its idle state or other status (upon
20 change or periodically, for example) or respond to a query
21 signal from a network device.

22 Also, in another embodiment, as shown in Figure 7, there
23 would be a (hardware/software and/or firmware and/or other
24 component) transponder device 21 resident in a part of the
25 network (such as network computer, switch, router, or another
26 PC, for examples) that receives 22 the PC device status
27 broadcast and/or queries 26 the PC for its status, as shown in

1 Figure 7.

2 In one embodiment, as shown in Figure 8, the network
3 would also have resident in a part of its hardware and/or
4 software (and/or firmware and/or other components) a capacity
5 such as to allow it to most effectively select and utilize the
6 available user PC's to perform parallel processing initiated
7 by PC users or the network providers or others. To do so, the
8 network should have the (hardware and/or software and/or
9 firmware and/or other component) capability of locating each
10 PC accurately at the PC's position on the geographic grid
11 lines/connection means 23 so that parallel processing occurs
12 between PC's (PC 1 and PC 1₂) as close together as possible,
13 which should not be difficult for PC's at fixed sites with a
14 geographic location, customarily grouped together into cells
15 24, as shown in Figure 8, but which requires an active system
16 for any wireless microprocessor to measure its distance from
17 its network relay site, as discussed below in Figure 14.

18 One of the primary capabilities of the Internet (or
19 Internet II or successor, like the MetaInternet) or WWW
20 network computer would be to facilitate searches by the PC
21 user or other user. As shown in Figure 9, searches are
22 particularly suitable to multiple processing, since, for
23 example, a typical search would be to find a specific Internet
24 or WWW site with specific information. Such site searches can
25 be broken up geographically, with a different PC processor 1'
26 allocated by the network communicating through a wired means
27 99 as shown (or wireless connections) to search each area, the

1 overall area being divided into eight separate parts, as
2 shown, which would preferably be about equal, so that the
3 total search would be about 1/8 as long as if one processor
4 did it alone (assuming the PC 1 microprocessor provides
5 control only and not parallel processing, which may be
6 preferable in some case).

7 As a typical example, a single PC user might need 1,000
8 minutes of search time to find what is requested, whereas the
9 network computer, using multiple PC processors, might be able
10 to complete the search in 100 minutes using 10 processors, or
11 10 minutes using 100 processors or 1 minute using 1,000
12 processors (or even 1 second using 60,000 processors);
13 assuming performance transparency, which should be achievable,
14 at least over time. The network's external parallel
15 processing is completely scalable, with virtually no
16 theoretical limit.

17 The above examples also illustrates a tremendous
18 potential benefit of network parallel processing. The same
19 amount of network resources, 60,000 processor seconds, was
20 expended in each of the equivalent examples. But by using
21 relatively large multiples of processors, the network can
22 provide the user with relatively immediate response with no
23 difference in cost (or relatively little difference) -- a
24 major benefit. In effect, each PC user linked to the network
25 providing external parallel processing becomes, in effect, a
26 virtual supercomputer! As discussed below, supercomputers
27 would experience a similar quantum leap in performance by

1 employing a thousand-fold (or more) increase in
2 microprocessors above current levels.

3 Such power will likely be required for any effective
4 searches in the World Wide Web (WWW). WWW is currently
5 growing at a rate such that it is doubling every year, so that
6 searching for information within the WWW will become
7 geometrically more difficult in future years, particularly a
8 decade hence, and it is already a very significant difficulty
9 to find WWW sites of relevance to any given search and then to
10 review and analyze the contents of the site.

11 So the capability to search with massive parallel
12 processing will be required to be effective and will
13 dramatically enhance the capabilities of scientific,
14 technological and medical researchers.

15 Such enhanced capabilities for searching (and analysis)
16 will also fundamentally alter the relationship of buyers and
17 sellers of any items and/or services. For the buyer, massive
18 parallel network processing will make it possible to find the
19 best price, worldwide, for any product or the most highly
20 rated product or service (for performance, reliability, etc.)
21 within a category or the best combination of price/performance
22 or the highest rated product for a given price point and so
23 on. The best price for the product can include best price for
24 shipping within specific delivery time parameters acceptable
25 to the buyer.

26 For the seller, such parallel processing will
27 drastically enhance the search, worldwide, for customers

1 potentially interested in a given product or service,
2 providing very specific targets for advertisement. Sellers,
3 even producers, will be able to know their customers directly
4 and interact with them directly for feedback on specific
5 products and services to better assess customer satisfaction
6 and survey for new product development.

7 Similarly, the vastly increased capability provided by
8 the system's shared parallel processing will produce major
9 improvements in complex simulations like modeling worldwide
10 and local weather systems over time, as well as design and
11 testing of any structure or product, from airliners and
12 skyscrapers, to new drugs and to the use of much more
13 sophisticated artificial intelligence (AI) in medical
14 treatment and in sorting through and organizing for PC users
15 the voluminous input of electronic data from "push"
16 technologies. Improvements in games would also be evident,
17 especially in terms of realistic simulation and interactivity.

18 As is clear from the examples, the Internet or WWW
19 network computer system like the MetaInternet would
20 potentially put into the hands of the PC user an extraordinary
21 new level of computer power vastly greater than the most
22 powerful supercomputer existing today. The world's total of
23 microchips is already about 350 billion, of which about 15
24 billion are microprocessors of some kind (most are fairly
25 simple "appliance" type running wrist watches, Televisions,
26 cameras, cars, telephones, etc). Assuming growth at its
27 current rates, in a decade the Internet/Internet II/WWW could

1 easily have a billion individual PC users, each providing a
2 average total of at least 10 highly sophisticated
3 microprocessors (assuming PC's with at least 4 microprocessors
4 (or more, such as 16 microprocessors or 32, for example) and
5 associated other handheld, home entertainment, and business
6 devices with microprocessors or digital processing capability,
7 like a digital signal processor or successor devices). That
8 would be a global computer a decade from now made of at least
9 10 billion microprocessors, interconnected by electromagnetic
10 wave means at speeds approaching the speed of light.

11 In addition, if the exceptionally numerous "appliance"
12 microprocessors noted above, especially those that operate now
13 intermittently like personal computers, are designed to the
14 same basic consensus industry standard as parallel
15 microprocessors for PC's (or equivalents or successors) or for
16 PC "systems on a chip" discussed later in Figure 10A-H, and if
17 also connected by broad bandwidth means such as fiber optic
18 cable or equivalent wireless, then the number of parallel
19 processors potentially available would increase roughly about
20 10 times, for a net potential "standard" computing performance
21 of up to 10,000 times current performance within fifteen
22 years, exclusive of Moore's Law routine increases. Moreover,
23 if all currently intermittently operating microprocessors
24 followed the same basic design standards, then although the
25 cost per microprocessor would rise somewhat, especially
26 initially, the net cost of computing for all users would fall
27 drastically due to the general performance increase due to the

1 use of otherwise idle "appliance" microprocessors. Overall
2 system costs will therefore compel such microprocessors, which
3 are currently specialty devices known as application-specific
4 integrated circuits (ASICs), virtually all to become general
5 microprocessors (like PC's), with software and firmware
6 providing most of their distinguishing functionality.

7 To put this in context, a typical supercomputer today
8 utilizing the latest PC microprocessors has less than a
9 hundred. Using network linkage to all external parallel
10 processing, a peak maximum of perhaps 1 billion
11 microprocessors could be made available for a network
12 supercomputer user, providing it with the power 10,000,000
13 times greater than would be available using today's internal
14 parallel processing supercomputers (assuming the same
15 microprocessor technology). Because of it's virtually
16 limitless scalability mentioned above, resources made
17 available by the network to the supercomputer user or PC user
18 would be capable of varying significantly during any computing
19 function, so that peak computing loads would be met with
20 effectively whatever level of resources are necessary.

21 In summary, regarding monitoring the net provision of
22 power between PC and network, Figures 1-9 show embodiments of
23 a system for a network of computers, including personal
24 computers, comprising: means for network services including
25 browsing functions, as well as shared computer processing such
26 as parallel processing, to be provided to the personal
27 computers within the network; at least two personal computers;

1 means for at least one of the personal computers, when idled
2 by a personal user, to be made available temporarily to
3 provide the shared computer processing services to the
4 network; and means for monitoring on a net basis the
5 provision of the services to each the personal computer or to
6 the personal computer user. In addition, Figures 1-9 show
7 embodiments including where the system is scalar in that the
8 system imposes no limit to the number of the personal
9 computers, including at least 1024 personal computers; the
10 system is scalar in that the system imposes no limit to the
11 number of personal computers participating in a single shared
12 computer processing operation, including at least 256 personal
13 computers; the network is connected to the Internet and its
14 equivalents and successors, so that the personal computers
15 include at least a million personal computers; the network is
16 connected to the World Wide Web and its successors; the
17 network includes at least one network server that participates
18 in the shared computer processing.; the monitoring means
19 includes a meter device to measure the flow of computing power
20 between the personal computers and the network; the monitoring
21 means includes a means by which the personal user of the
22 personal computer is provided with a prospective estimate of
23 cost for the network to execute an operation requested by the
24 personal user prior to execution of the operation by the
25 network; the system has a control means by which to permit and
26 to deny access to the personal computers by the network for
27 shared computer processing; access to the personal computers

1 by the network is limited to those times when the personal
2 computers are idle; and the personal computers having at least
3 one microprocessor and communicating with the network through
4 a connection means having a speed of data transmission that is
5 at least greater than a peak data processing speed of the
6 microprocessor.

7 Also, relative to maintaining a standard cost, Figures
8 1-9 show embodiments of a system for a network of computers,
9 including personal computers, comprising: means for network
10 services including browsing functions, as well as shared
11 computer processing such as parallel processing, to be
12 provided to the personal computers within the network; at
13 least two personal computers; means for at least one of the
14 personal computers, when idled by a personal user, to be made
15 available temporarily to provide the shared computer
16 processing services to the network; and means for maintaining
17 a standard cost basis for the provision of the services to
18 each personal computer or to the personal computer user. In
19 addition, Figures 1-9 show embodiments including where the
20 system is scalar in that the system imposes no limit to the
21 number of personal computers, including at least 1,024
22 personal computers; the system is scalar in that the system
23 imposes no limit to the number of the personal computers
24 participating in a single shared computer processing
25 operation, including at least 256 personal computers; the
26 network is connected to the Internet and its equivalents and
27 successors, so that the personal computers include at least a

1 million personal computers; the standard cost is fixed; the
2 fixed standard cost is zero; the means for maintaining a
3 standard cost basis includes the use of making available a
4 standard number of personal computers for shared processing by
5 personal computers; the network is connected to the World Wide
6 Web and its successors; the personal user can override the
7 means for maintaining a standard cost basis so that the
8 personal user can obtain additional network services; the
9 system has a control means by which to permit and to deny
10 access to the personal computers by the network for shared
11 computer processing; the personal computers having at least
12 one microprocessor and communicating with the network through
13 a connection means having a speed of data transmission that is
14 at least greater than a peak data processing speed of the
15 microprocessor.

16 Browsing functions generally include functions like
17 those standard functions provided by current Internet
18 browsers, such as Microsoft Explorer 3.0 or 4.0 and Netscape
19 Navigator 3.0 or 4.0, including at least searching World Wide
20 Web or Internet sites, exchanging E-Mail worldwide, and
21 worldwide conferencing; an intranet network uses the same
22 browser software, but might not include access to the Internet
23 or WWW. Shared processing includes at least parallel
24 processing and multitasking processing involving more than two
25 personal computers, as defined above. The network system is
26 entirely scalar, with any number of PC microprocessors
27 potentially possible.

1 As shown in Figures **10A-10F**, to deal with operational
2 and security issues, it may be especially useful for
3 individual PC users to have one microprocessor or equivalent
4 device that is designated, permanently or temporarily, to be a
5 master 30 controlling device (comprised of hardware and/or
6 software and/of firmware and/or other component) that remains
7 unaccessible (preferably using a hardware and/or software
8 and/or firmware and/or other component firewall 50) directly
9 by the network but which controls the functions of the other,
10 slave microprocessors 40 when is not utilizing them.

11 For example, as shown in Figures **10A**, a typical PC 1
12 might have four or five microprocessors (even on a single
13 microprocessor chip), with one master 30 and three or four
14 slaves 40, depending on whether the master 30 is a controller
15 exclusively (through different design of any component part),
16 requiring four slave microprocessors 40 preferably; or the
17 master microprocessor 30 has the same or equivalent
18 microprocessing capability as a slave 40 and multiprocesses in
19 parallel with the slave microprocessors 40, thereby requiring
20 only three slave microprocessors 40, preferably. The number
21 of PC slave microprocessors 40 can be increased to virtually
22 any other number, such as at least about eight, about 16,
23 about 32, about 64, about 128, about 256, about 512, about
24 1024, and so on (these specific multiples are preferred, but
25 not required; the PC master microprocessors 30 can also be
26 increased). Also included is at least one preferred firewall
27 50 between master 30 and slave 40 microprocessors. As shown

1 in preceding Figures 1-9, the PC 1 in Figure 10A is preferably
2 connected to a network computer 2 and to the Internet or WWW
3 or present or future equivalent or successor 3, like the
4 MetaInternet.

5 Other typical PC hardware components such as hard drive
6 61, floppy diskette 62, compact disk-read only memory (CD-ROM)
7 63, digital video disk (DVD) 64, Flash memory 65, random
8 access memory (RAM) 66, video or other display 67, graphics
9 card 68, and sound card 69, as well as digital signal
10 processor or processors, together with the software and/or
11 firmware stored on or for them, can be located on either side
12 of the preferred firewall 50, but such devices as the display
13 67, graphics card 68 and sound card 69 and those devices that
14 both read and write and have non-volatile memory (retain data
15 without power and generally have to be written over to erase),
16 such as hard drive 62, Flash memory 65, floppy drive 62,
17 read/write CD-ROM 63 or DVD 64 are preferred to be located on
18 the PC user side of the firewall 50, where the master
19 microprocessor is also located, as shown in Figure 10A, for
20 security reasons primarily; their location can be flexible,
21 with that capability controlled such as by password-authorized
22 access.

23 Alternately, any or these devices that are duplicative
24 (or for other exceptional needs) like a second hard drive 61'
25 can be located on the network side of the firewall 50. RAM 66
26 or equivalent or successor memory, which typically is volatile
27 (data is lost when power is interrupted), should generally be

1 located on the network side of the firewall 50, however some
2 can be located with the master microprocessor to facilitate
3 its independent use.

4 Read-only memory devices such as most current CD drives
5 (CD-ROM's) 63' or DVD's (DVD-ROM) 64' can be safely located on
6 the network side of the firewall 50, since the data on those
7 drives cannot be altered by network users; preemptive control
8 of use would preferably remain with the PC user in terms of
9 interrupting network use.

10 However, at least a portion of RAM is can be kept on the
11 Master 30 microprocessor side of the firewall 50, so that the
12 PC user can use retain the ability to use a core of user PC 1
13 processing capability entirely separate from any network
14 processing; if this capability is not desired, then the master
15 30 microprocessor can be moved to the network side of the
16 firewall 50 and replaced with a simpler controller on the PC 1
17 user side, like the master remote controller 31 discussed
18 below and shown in Figure 10I.

19 And the master microprocessor 30 might also control the
20 use of several or all other processors 60 owned or leased by
21 the PC user, such as home entertainment digital signal
22 processors 70, especially if the design standards of such
23 microprocessors in the future conforms to the requirements of
24 network parallel processing as described above. In this
25 general approach, the PC master processor would use the slave
26 microprocessors or, if idle (or working on low priority,
27 deferable processing), make them available to the network

1 provider or others to use. Preferably, wireless connections
2 100 would be extensively used in home or business network
3 systems, including use of a master remote controller 31
4 without (or with) microprocessing capability, with preferably
5 broad bandwidth connections such as fiber optic cable
6 connecting directly to at least one component such as a PC 1,
7 shown in a slave configuration, of the home or business
8 personal network system; that preferred connection would link
9 the home system to the network 2 such as the Internet 3, as
10 shown in Figure 10I. A business system would include
11 preferably fiber optic links to most or all personal computers
12 PC 1 and other devices with microprocessors, such as printers,
13 copiers, scanners, fax machines, telephone and video
14 conferencing equipment; wireless links can be used also.

15 A PC 1 user can remotely access his networked PC 1 by
16 using another networked master microprocessor 30 on another PC
17 1 and using a password or other access control means for entry
18 to his own PC 1 master microprocessor 30 and files, as is
19 common now in Internet and other access. Alternately, a
20 remote user can simply carry his own files and his own master
21 microprocessor or use another networked master microprocessor
22 temporarily has his own.

23 In the simplest multi-microprocessor configuration, as
24 shown in Figure 10B, the PC 1 would have a single master
25 microprocessor 30 and a single slave microprocessor 40,
26 preferably separated by a firewall 50, with both processors
27 used in parallel or multitasking processing or with only the

1 slave 40 so used, and preferably connected to a network
2 computer 2 and Internet 3 (and successors like the
3 MetaInternet). Virtually any number of slave microprocessors
4 40 is possible. The other non-microprocessor components shown
5 in Figure 10A above might also be included in this simple
6 Figure 10B configuration.

7 Preferably, as shown in Figure **10C**, single chip
8 microprocessors 90 can integrate most or all of the other
9 necessary computer components (or their present or future
10 equivalents or successors), like a PC's memory (RAM 66,
11 graphics 82, sound 83, power management 84, network
12 communications 85, and video processing 86, possibly including
13 modem 87, flash bios 88, digital signal processor or
14 processors 89, and other components or present or future
15 equivalents or successors) and internal bus, on a single chip
16 90 (silicon, plastic, or other), known in the industry as a
17 "system on a chip". Such a PC micro chip 90 would preferably
18 have the same architecture as that of the PC 1 shown above in
19 Figure 10A: namely, a master control and/or processing unit 93
20 and one or more slave processing units 94 (for parallel or
21 multitasking processing by either the PC 1 or the Network 2),
22 preferably separated by a firewall 50 and preferably connected
23 to a network computer 3 and the Internet 3 and successors like
24 the MetaInternet.

25 Existing PC components with mechanical components like
26 hard drive 61, floppy or other removable diskette 62, CD-ROM
27 63 and DVD 64, which are mass storage devices with mechanical

1 features that will likely not become an integral part of a PC
2 "system of a chip" would preferably, of course, still be
3 capable of connection to a single PC micro chip 90 and control
4 by a single PC master unit 93.

5 In the simplest multi-processor case, as shown in Figure
6 **10D**, the chip 90 would have a single master unit 93 and at
7 least one slave unit 94 (with the master having a controlling
8 function only or a processing function also), preferably
9 separated by a firewall 50 and preferably connected to a
10 network computer 3 and the Internet 3 (and successors like the
11 MetaInternet). The other non-microprocessor components shown
12 in Figure 10A above might also be included in this simple
13 Figure 10D configuration.

14 As noted in the second paragraph of the introduction to
15 the background of the invention, in the preferred network
16 invention, any computer can potentially be both a user and
17 provider, alternatively -- a dual mode operating capability.

18 Consequently, any PC 1 within the network 2, preferably
19 connected to the Internet 3 (and successors like the
20 MetaInternet), can be temporarily a master PC 30 at one time
21 initiating a parallel or multitasking processing request to
22 the network 2 for execution by at least one slave PC 40, as
23 shown in Figure **10E**. At another time the same PC 1 can become
24 a slave PC 40 that executes a parallel or multitasking
25 processing request by another PC 1' that has temporarily
26 assumed the function of master 30, as shown in Figure **10F**.
27 The simplest approach to achieving this alternation is for

1 both master and slave versions of the parallel processing
2 software to be loaded in each or every PC 1 that is to share
3 in the parallel processing, so each PC 1 has the necessary
4 software means, together with minor operational modifications,
5 such as adding a switching means by which a signaled request
6 for parallel processing initiated by one PC 1 user using
7 master software is transmitted to at least a second PC 1,
8 triggering its slave software to respond by initiating
9 parallel processing.

10 As shown in Figures **10G** and **10H**, which are parallel to
11 Figures 10E and 10F, the number of PC slave processors 40 can
12 be increased to any virtually other number, such as at least
13 about 4, as shown; the design of the processing system is
14 completely scalar, so that further increases can occur to
15 about eight slave microprocessors 40, about 16, about 32,
16 about 64, about 128, about 256, about 512, about 1024, and so
17 on (these multiples indicated are preferred, not required);
18 the PC master microprocessors 30 can also be increased.

19 As noted above relative to Figure 10I, a PC 1 can
20 function as a slave PC 40 and be controlled by a master
21 controller 31, which can be remote and which may have limited
22 or no microprocessing capability. As shown in Figure **10J** and
23 **10K**, such a master controller 31 would be located on the PC
24 user side of the firewall 50, under the control of the PC
25 user, while the microprocessors 40 would reside on the network
26 side of the firewall 50. The master controller 31 preferably
27 would receive input from the PC user by any user/PC 1

1 interface means such as keyboard, microphone, videocam or
2 future hardware and/or software and/or firmware or other
3 equivalent or successor interface means (as would a master
4 processor 40) that provides input to a PC 1 or microprocessor
5 30 originating from a user's hand, voice, eye, nerve or
6 nerves, or other body part; in addition, remote access might
7 also be enabled by a hardware and/or software and/or firmware
8 and/or other means with suitable security such as password
9 controlled access. Similarly, as shown in Figure **10L** and **10M**,
10 relative to a PC "system on a chip" a master controller unit
11 93' (which could be capable of being accessed by the PC user
12 through a remote controller 31) with only a controlling
13 capability would be located on the PC user side of the
14 firewall 50, under the control of the PC user, while the slave
15 processor units 94 would reside on the network side of the
16 firewall 50.

17 Figures **10N** and **10O** show PC 1 with a firewall 50 that is
18 configurable through either hardware and/or software and/or
19 firmware and/or other means; software configuration would be
20 easiest and most typical, but active motherboard configuration
21 is possible and may present some security advantages; manual
22 switches could of course be used potentially. Figure 10N
23 shows a CD-ROM 63' that has been placed by a PC user on the
24 network side of a firewall 50 from a previous position on the
25 PC user side of a firewall 50, which was shown in Figure 10A.
26 Preferably, the settings of a firewall 50 would default to
27 those that would most safely protect the PC 1 from

1 uncontrolled access by network users, but with capability for
2 the relatively sophisticated PC user to override such default
3 settings, but with proper safeguards to protect the
4 unsophisticated user from inadvertently doing so;
5 configuration of a firewall 50 might also be actively
6 controlled by a network administrator in a local network like
7 that of a business, where a PC user may not be owner or leaser
8 of the PC being used.

9 Similarly, Figures 10P and 10Q show a PC "system of a
10 chip" 90 with a firewall 50 that is configurable through
11 either hardware and/or software and/or firmware and/or other
12 means; software configuration would be easiest and most
13 typical. Active configuration of the integrated circuits of
14 the PC microchip 90 is also possible and may present some
15 speed and security advantages. Such direct configuration of
16 the circuits of the microchip 90 to establish or change in its
17 firewall 50 could be provided by the use of field-programmable
18 gate arrays (or FPGA's) or their future equivalents or
19 successors; in Figure 10P, for example, slave processing unit
20 94' has been moved to the PC user side of a firewall 50 from a
21 network side position shown in Figure 10C and 10L. Similarly,
22 Figure 10Q shows the same active configuration of chip circuit
23 using FPGA's for the simplest form of multiprocessing
24 microchip 90 with a single slave unit 94', transferring its
25 position to the PC user's side of a firewall 50 from a network
26 side shown in Figure 10M and 10D.

27 In summary, relative to the use of master/slave

1 computers, Figures 10A-10I show embodiments of a system for a
2 network of computers, including personal computers,
3 comprising: at least two personal computers; means for at
4 least one personal computer, when directed by its personal
5 user, to function temporarily as a master personal computer to
6 initiate and control the execution of a computer processing
7 operation shared with at least one other personal computer in
8 the network; means for at least one other personal computer,
9 when idled by its personal user, to be made available to
10 function temporarily as at least one slave personal computer
11 to participate in the execution of a shared computer
12 processing operation controlled by the master personal
13 computer; and means for the personal computers to alternate as
14 directed between functioning as a master and functioning as a
15 slave in the shared computer processing operations. In
16 addition, Figures 10A-10I show embodiments including wherein
17 the system is scalar in that the system imposes no limit to
18 the number of personal computers; the system includes at least
19 256 said personal computers; the system is scalar in that the
20 system imposes no limit to the number of personal computers
21 participating in a single shared computer processing
22 operation, including at least 256 said personal computers; the
23 system is scalar in that the system imposes no limit to the
24 number of personal computers participating in a single shared
25 computer processing operation, including at least 256 said
26 personal computers; the network is connected to the Internet
27 and its equivalents and successors, so that personal computers

1 include at least a million personal computers; the shared
2 computer processing is parallel processing; the network is
3 connected to the World Wide Web and its successors; a means
4 for network services, including browsing and broadcast
5 functions, as well as shared computer processing such as
6 parallel processing, are provided to said personal computers
7 within said network; the network includes at least one network
8 server that participates in the shared computer processing;
9 the personal computers include a transponder means so that a
10 master personal computer can determine the closest available
11 slave personal computers; the closest available slave personal
12 computer is compatible with the master personal computer to
13 execute said shared computer processing operation; the
14 personal computers having at least one microprocessor and
15 communicating with the network through a connection means
16 having a speed of data transmission that is at least greater
17 than a peak data processing speed of the microprocessor; and a
18 local network PC 1 being controlled remotely by a
19 microprocessor controller 31.

20 The preferred use of the firewall 50, as described above
21 in Figures 10A-10I, provides a solution to an important
22 security problem by preferably completely isolating host PC's
23 1 that are providing slave microprocessors to the network for
24 parallel or other shared processing functions from any
25 capability to access or retain information about any element
26 about that shared processing. In addition, of course, the
27 firewall 50 provides security for the host PC against

1 intrusion by outside hackers; by reducing the need for
2 encryption and authentication, the use of firewalls 50 will
3 provide a relative increase in computing speed and efficiency.

4 In addition to computers such as personal computers, the
5 firewall 50 described above could be used in any device with
6 "appliance"-type microprocessors, such as telephones,
7 televisions or cars, as discussed above.

8 In summary, regarding the use of firewalls, Figures 10A-
9 10I show embodiments of a system architecture for computers,
10 including personal computers, to function within a network of
11 computers, comprising: a computer with at least two
12 microprocessors and having a connection means with a network
13 of computers; the architecture for the computers including a
14 firewall means for personal computers to limit access by the
15 network to only a portion of the hardware, software, firmware,
16 and other components of the personal computers; the firewall
17 means will not permit access by the network to at least a one
18 microprocessor having a means to function as a master
19 microprocessor to initiate and control the execution of a
20 computer processing operation shared with at least one other
21 microprocessor having a means to function as a slave
22 microprocessor; and the firewall means permitting access by
23 the network to the slave microprocessor. In addition, the
24 system architecture explicitly includes embodiments of, for
25 example, the computer is a personal computer; the personal
26 computer is a microchip; the computer have a control means by
27 which to permit and to deny access to the computer by the

1 network for shared computer processing; the system is scalar
2 in that the system imposes no limit to the number of personal
3 computers, including at least 256 said personal computers; the
4 network is connected to the Internet and its equivalents and
5 successors, so that the personal computers include at least a
6 million personal computers; the system is scalar in that the
7 system imposes no limit to the number of personal computers
8 participating in a single shared computer processing
9 operation, including at least 256 said personal computers; the
10 personal computers having at least one microprocessor and
11 communicating with the network through a connection means
12 having a speed of data transmission that is at least greater
13 than a peak data processing speed of the microprocessor.

14 In summary, regarding the use of controllers with
15 firewalls, Figures 10J-10M show embodiments of a system
16 architecture for computers, including personal computers, to
17 function within a network of computers, comprising: a computer
18 with at least a controller and a microprocessor and having a
19 connection means with a network of computers; the architecture
20 for the computers including a firewall means for personal
21 computers to limit access by the network to only a portion of
22 the hardware, software, firmware, and other components of the
23 personal computers; the firewall means will not permit access
24 by the network to at least a one controller having a means to
25 initiate and control the execution of a computer processing
26 operation shared with at least one microprocessor having a
27 means to function as a slave microprocessor; and the firewall

1 means permitting access by the network to the slave
2 microprocessor. In addition, the system architecture
3 explicitly includes embodiments of, for example, the computer
4 is a personal computer; the personal computer is a microchip;
5 the computer have a control means by which to permit and to
6 deny access to the computer by the network for shared computer
7 processing; the system is scalar in that the system imposes no
8 limit to the number of personal computers, including at least
9 256 said personal computers; the network is connected to the
10 Internet and its equivalents and successors, so that the
11 personal computers include at least a million personal
12 computers; the system is scalar in that the system imposes no
13 limit to the number of personal computers participating in a
14 single shared computer processing operation, including at
15 least 256 said personal computers; the personal computers
16 having at least one microprocessor and communicating with the
17 network through a connection means having a speed of data
18 transmission that is at least greater than a peak data
19 processing speed of the microprocessor; and the controller
20 being capable of remote use.

21 In summary, regarding the use of firewalls that can be
22 actively configured, Figures 10N-10Q show embodiments of a
23 system architecture for computers, including personal
24 computers, to function within a network of computers,
25 comprising: a computer with at least two microprocessors and
26 having a connection means with a network of computers; the
27 architecture for the computers including a firewall means for

1 personal computers to limit access by the network to only a
2 portion of the hardware, software, firmware, and other
3 components of the personal computers; the firewall means will
4 not permit access by the network to at least a one
5 microprocessor having a means to function as a master
6 microprocessor to initiate and control the execution of a
7 computer processing operation shared with at least one other
8 microprocessor having a means to function as a slave
9 microprocessor; the firewall means permitting access by the
10 network to the slave microprocessor; the configuration of the
11 firewall being capable of change by a user or authorized local
12 network administrator; the change in firewall configuration of
13 a microchip PC is made at least in part using field-
14 programmable gate arrays or equivalents or successors. In
15 addition, the system architecture explicitly includes
16 embodiments of, for example, the computer is a personal
17 computer; the personal computer is a microchip; the computer
18 have a control means by which to permit and to deny access to
19 the computer by the network for shared computer processing;
20 the system is scalar in that the system imposes no limit to
21 the number of personal computers, including at least 256 said
22 personal computers; the network is connected to the Internet
23 and its equivalents and successors, so that the personal
24 computers include at least a million personal computers; the
25 system is scalar in that the system imposes no limit to the
26 number of personal computers participating in a single shared
27 computer processing operation, including at least 256 said

1 personal computers; the personal computers having at least one
2 microprocessor and communicating with the network through a
3 connection means having a speed of data transmission that is
4 at least greater than a peak data processing speed of the
5 microprocessor.

6 It is presently contemplated that PC 1 microprocessors
7 noted above be designed to the same basic consensus industry
8 standard as parallel microprocessors for PC's (or equivalents
9 or successors) as in Figures 10A-10B or for PC "systems on a
10 chip" discussed in Figures 10C-10D. Although the cost per
11 microprocessor might rise somewhat initially, the net cost of
12 computing for all users would fall drastically almost
13 instantly due to the significant general performance increase
14 created by the new capability to use of heretofore idle
15 "appliance" microprocessors. The high potential for very
16 substantial benefit to all users should provide a powerful
17 force to reach consensus on important industry hardware,
18 software, and other standards on a continuing basis for such
19 basic parallel network processing designs utilizing the
20 Internet 3 and successor. It is presently contemplated that
21 such basic industry standards be adopted at the outset and for
22 use of only the least number of shared microprocessors
23 initially. As design improvements incorporating greater
24 complexity and more shared microprocessors are phased in
25 gradually overtime on a step by step basis, then conversion to
26 a MetaInternet architecture at all component levels should be
27 relatively easy and inexpensive (whereas an attempt at sudden,

1 massive conversion would be hugely difficult and prohibitively
2 expensive). The scalability of the MetaInternet system
3 architecture (both vertically and horizontally) as described
4 herein makes this sensible incremental approach possible.

5 By 1998, manufacturing technology improvements will
6 allow as many as 20 million transistors to fit on a single
7 chip (with circuits as thin as .25 microns) and, in the next
8 cycle, 50 million transistors using .18 micron circuits.
9 Preferably, that entire computer on a chip would be linked,
10 preferably directly, by fiber optic or other broad bandwidth
11 connection means to the network so that the limiting factor on
12 data throughput in the network system, or any part, is only
13 the speed of the linked microprocessors themselves, not the
14 transmission speed of the linkage. Such direct fiber optic
15 linkage will obviate the need for an increasingly unwieldy
16 number of microchip connection prongs, which is currently in
17 the one to two hundred range in the Intel Pentium series and
18 will reach over a thousand prongs in the 1998 IBM Power3
19 microprocessor. One or more digital signal processors 89
20 located on a microprocessor, together with numerous channels
21 and/or signal multiplexing of the fiber optic signal can
22 substitute for a vast multitude of microchip connection
23 prongs.

24 For computers that are not reduced to a single chip, it
25 is also preferred that the internal system bus or buses of any
26 such PC's have a transmission speed that is at least high
27 enough that the all processing operations of the PC

1 microprocessor or microprocessors is unrestricted (and other
2 PC components like RAM) and that the microprocessor chip or
3 chips are directly linked by fiber optic or other broad
4 bandwidth connection, as with the system chip described above,
5 so that the limiting factor on data throughput in the network
6 system, or any part, is only the speed of the linked
7 microprocessors themselves, not the transmission speed of the
8 linkage.

9 The individual user PC's can be connected to the
10 Internet (via an Intranet)/Internet II/WWW or successor, like
11 the MetaInternet (or other) network by any electromagnetic
12 means, with the speed of fiber optic cable being preferred,
13 but hybrid systems using fiber optic cable for trunk lines and
14 coaxial cable to individual users may be more cost effective
15 initially, but much less preferred unless cable can be made
16 (through hardware and/or software and/or firmware and/or other
17 component means) to provide sufficiently broad bandwidth
18 connections to provide unrestricted throughput by connected
19 microprocessors. Given the speed and bandwidth of
20 transmission of fiber optic or equivalent connections,
21 conventional network architecture and structures should be
22 acceptable for good system performance, making possible a
23 virtual complete interconnection network between users.

24 However, the best speed for any parallel processing
25 operation should be obtained, all other things being equal, by
26 utilizing the available microprocessors that are physically
27 the closest together. Consequently, as shown previously in

1 Figure 8, the network needs have the means (through hardware
2 and/or software and/or firmware and/or other component) to
3 provide on a continually ongoing basis the capability for each
4 PC to know the addresses of the nearest available PC's,
5 perhaps sequentially, from closest to farthest, for the area
6 or cell immediately proximate to that PC and then those cells
7 of adjacent areas.

8 Network architecture that clusters PC's together should
9 therefore be preferred and can be constructed by wired means.

10 However, as shown in Figure 11, it would probably be very
11 beneficial to construct local network clusters 101 (or cells)
12 of personal computers 1' by wireless 100 means, since physical
13 proximity of any PC 1 to its closest other PC 1' should be
14 easier to access directly that way, as discussed further
15 below. Besides, it is economically preferable for at least
16 several network providers to serve any given geographic area
17 to provide competitive service and prices.

18 It would be advantageous, then, for those wireless PC
19 connections to be PC resident and capable of communicating by
20 wireless or wired (or mixed) means with all available PC's in
21 the cluster or cell geographic area, both proximal and
22 potentially out to the practical limits of the wireless
23 transmission.

24 As shown in Figure 12, wireless PC connections 100 can
25 be made to existing non-PC network components, such as one or
26 more satellites 110, or present or future equivalent or
27 successor components and the wireless transmissions can be

1 conventional radio waves, such as infrared or microwave, or
2 can utilize any other part of the electromagnetic wave
3 spectrum.

4 Moreover, as shown in Figure 13, such a wireless or
5 wired (or mixed) approach would also make it easily possible
6 in the future to develop network clusters 101 of available
7 PC's 1' with complete interconnectivity; i.e., each available
8 PC 1 in the cluster 101 is directly connected (shown
9 wirelessly 100) to every other available PC 1 in the cluster
10 101, constantly adjusting to individual PC's becoming
11 available or unavailable. Given the speed of some wired broad
12 bandwidth connections, like fiber optic cable, such clusters
13 101 with complete interconnectivity is certainly a possible
14 embodiment.

15 As shown in Figure 14A-14D, it would be advantageous for
16 such wireless systems to include a wireless device 120
17 comprised of hardware and/or software and/or firmware and/or
18 other component, like the PC 1 availability device described
19 above preferably resident in the PC, but also with a network-
20 like capability of measuring the distance from each PC 1 in
21 its cluster 101 by that PC's signal transmission by
22 transponder or its functional equivalent and/or other means to
23 the nearest other PC's 1' in the cluster 101. As shown in
24 Figure 14A, this distance measurement could be accomplished in
25 a conventional manner between transponder devices 120
26 connected to each PC in the cluster 101; for example, by
27 measuring in effect the time delay from wireless transmission

1 by the transponder device 120 of an interrogating signal 105
2 to request initiation of shared processing by a master PC 1 to
3 the reception of a wireless transmission response 106
4 signaling availability to function as a slave PC from each of
5 the idle PC's 1' in the cluster 101 that has received the
6 interrogation signal 105. The first response signal 106'
7 received by the master PC 1 would be from the closest
8 available slave PC 1" (assuming the simplest shared processing
9 case of one slave PC and one master PC), which would be
10 selected for the shared processing operation by the requesting
11 master PC 1, since the closer the shared microprocessor, the
12 faster the speed of the wireless connections 100 would be
13 between sharing PC's (assuming equivalence of the connection
14 means and other components among each of the PC's 1'). The
15 interrogation signal 105 might specify other selection
16 criteria also, for example, for the closest compatible
17 (initially perhaps defined by a functional requirement of the
18 system to be an identical microprocessor) slave PC 1", with
19 the first response signal 106' being selected as above.

20 This same transponder approach also can be used between
21 PC's 1" connected by a wired 99 (or mixed wired/wireless)
22 means, despite the fact that connection distances would
23 generally be greater (since not line of sight, as is
24 wireless), as shown in Figure 14A, since the speed of
25 transmission by the preferred broad bandwidth transmission
26 means such as fiber optic cable is so high as to offset that
27 greater distance. From a cost basis, this wired approach

1 might be preferable for such PC's already connected by broad
2 bandwidth transmission means, since additional wireless
3 components like hardware and software would not be necessary.

4 In that case, a functionally equivalent transponder device
5 120 would preferably be operated in wired clusters 101 in
6 generally the same manner as described above for PC's
7 connected in wireless clusters 101. Networks incorporating
8 PC's 1 connected by both wireless and wired (or mixed) means
9 are anticipated, like the home or business network mentioned
10 in Figure 10I, with mobile PC's or other computing devices
11 preferably using wireless connections. Depending on distances
12 between PC's and other factors, a local cluster 101 of a
13 network 2 might connect wirelessly between PC's and with the
14 network 2 through transponding means linked to wired broad
15 bandwidth transmission means, as shown in Figure 14C.

16 As shown in Figure 14D, the same general transponder
17 device means 120 can also be used in a wired 99 network system
18 2 employing network servers 98 operated, for example, by an
19 ISP, or in any other network system architectures (including
20 client/server or peer to peer) or any other topologies
21 (including ring, bus, and star) either well known now in the
22 art or their future equivalents or successors.

23 The Figure 14 approach to establishing local PC clusters
24 101 for parallel or other shared processing has major
25 advantage in that it avoids using network computers such as
26 servers (and, if wireless, other network components including
27 even connection means), so that the entire local system of

1 PC's within a cluster 101 would operate independently of
2 network servers, routers, etc. Moreover, particularly if
3 connected by wireless means, the size of the cluster 101 could
4 be quite large, being limited generally by PC wireless
5 transmission power, PC wireless reception sensitivity, and
6 local and/or other conditions affecting transmission and
7 reception. Additionally, one cluster 101 could communicate by
8 wireless 100 means with an adjacent or other clusters 101, as
9 shown in Figure 14B, which could thereby include those beyond
10 its own direct transmission range.

11 To improve response speed in shared processing involving
12 a significant number of slave PC's 1, a virtual potential
13 parallel processing network for PC's 1 in a cluster 101 would
14 preferably be established before a processing request begins.

15 This would be accomplished by the transponder device 120 in
16 each idle PC 1, a potential slave, broadcasting by transponder
17 120 its available state when it becomes idle and/or
18 periodically afterwards, so that each potential master PC 1 in
19 the local cluster 101 would be able to maintain relatively
20 constantly its own directory 121 of the idle PC's 1 closest to
21 it that are available to function as slaves. The directory
22 121 would contain, for example, a list of about the standard
23 use number of slave PC's 1 for the master PC (which initially
24 would probably be just one other PC 1") or a higher number,
25 preferably listed sequentially from the closest available PC
26 to the farthest. The directory of available slave PC's 1
27 would be preferably updated on a relatively up to date basis,

1 either when a change occurs in the idle state of a potential
2 slave PC in the directory 121 or periodically.

3 Such ad hoc clusters 101 should be more effective by
4 being less arbitrary geographically, since each individual PC
5 would be effectively in the center of its own ad hoc cluster.

6 Scaling up or down the number of microprocessors required by
7 each PC at any given time would also be more seamless.

8 The complete interconnection potentially provided by
9 such highly effective ad hoc wireless clusters is also
10 remarkable because such clusters mimics the neural network
11 structure of the human brain, wherein each nerve cell, called
12 a neuron, interconnects in a very complicated way with the
13 neurons around it. By way of comparison, the global network
14 computer described above that is expected in a decade will
15 have at least about 10 times as many PC 's as a human brain
16 has neurons and they will be connected by electromagnetic
17 waves traveling at close to the speed of light, which is about
18 300,000 times faster than the transmission speed of human
19 neurons (which, however, will be much closer together).

20 An added note: in the next decade, as individual PC's
21 become much more sophisticated and more network oriented,
22 compatibility issues may recede to unimportance, as all major
23 types of PC's will be able to emulate each other and most
24 software, particularly relative to parallel processing, will
25 no longer be hardware specific. Nearer term it will be
26 important to set compatible hardware, software, firmware, and
27 other component standards to achieve substantial performance

1 advantages for the components of the global network computer.

2 Until that compatibility is designed into the essential
3 components of network system, the existing incompatibility of
4 current components dramatically increase the difficulty
5 involved in parallel processing across large networks.
6 Programming languages like Java is one approach that will
7 provide a partial means for dealing with this interim problem.

8 In addition, using similar configurations of existing
9 standards, like using PC's with a specific Intel Pentium chip
10 with other identical or nearly identical components is
11 probably the best way in the current technology to eliminate
12 many of the serious existing problems that could easily be
13 designed around in the future by adopting reasonable consensus
14 standards for specification of all system components. The
15 potential gains to all parties with an interest far outweigh
16 the potential costs.

17 The above described global network computer system has
18 an added benefit of reducing the serious and growing problem
19 of the nearly immediate obsolescence of computer hardware,
20 software, firmware, and other components. Since the preferred
21 system above is the sum of its constituent parts used in
22 parallel processing, each specific PC component becomes less
23 critical. As long as access to the network utilizing
24 sufficient bandwidth is possible, then all other technical
25 inadequacies of the user's own PC will be completely
26 compensated for by the network's access to a multitude of
27 technically able PC's of which the user will have temporary

1 use.

2 Although the global network computer will clearly cross
3 the geographical boundaries of nations, its operation should
4 not be unduly bounded by inconsistent or arbitrary laws within
5 those states. There will be considerable pressure on all
6 nations to conform to reasonable system architecture and
7 operational standards generally agreed upon, since the penalty
8 of not participating in the global network computer is
9 potentially so high as to not be politically possible
10 anywhere.

11 As shown in Figure 15, because the largest number of
12 user PC's will be completely idle, or nearly so, during the
13 night, it would be highly effective for the most complicated
14 large scale parallel processing, involving the largest numbers
15 of processors with uninterrupted availability as close
16 together as possible, to be routed by the network to
17 geographic areas of the globe undergoing night and to keep
18 them there even as the Earth rotates by shifting computing
19 resources as the world turns. As shown in the simplest case
20 in Figure 15, during the day, at least one parallel processing
21 request by at least one PC 1 in a network 2 in the Earth's
22 western hemisphere 131 are transmitted by very broad bandwidth
23 connection wired 99 means such as fiber optic cable to the
24 Earth's eastern hemisphere 132 for execution by at least one
25 PC 1' of a network 2', which is idle during the night and the
26 results are transmitted back by the same means to network 2
27 and the requesting at least one PC 1. Any number of

1 individual PC's within local networks like that operated by an
2 ISP could be grouped into clusters or cells, as is typical in
3 the practice of network industries. As is common in operating
4 electrical power grids and telecommunications and computer
5 networks, many such processing requests from many PC's and
6 many networks could be so routed for remote processing, with
7 the complexity of the system growing substantially over time
8 in a natural progression.

9 While the conventional approach to configuring a network
10 of personal computers PC 1 for parallel processing is simply
11 to string them together serially, as shown previously in
12 Figure 9, new Figures 16A-16Z and 16AA show a new hierarchial
13 network topology.

14 Although the Figure 9 network structure is simple and
15 produces reasonable results in loosely coupled problems like
16 geographic searches described earlier, as a general approach
17 it has at least three important problems.

18 First, a great deal of complex pre-operation planning
19 and custom tailoring-type programming at the master PC 1 level
20 is require to establish a means for allocating portions of the
21 operation among some number of available personal computers PC
22 1'.

23 Second, operations results coming back from personal
24 computers PC 1' are not synchronized, so that PC 1 frequently
25 alternates between being idle and being overwhelmed. When the
26 number of personal computers PC 1' is very large, both
27 problems can be significant.

1 Third, generally there is no means established for
2 personal computers PC 1' to communicate or cooperate with each
3 other during operations, so sharing operational results during
4 processing between personal computers PC 1' is not feasible.
5 Consequently, closely coupled problems are generally not
6 amenable to solution by conventional parallel processing by
7 computers.

8 The new hierarchical network topology shown in Figure
9 16A is a simple subdivision step whereby a personal computer
10 PC 1 (or microprocessor 30) acting as a master M_1 divides a
11 given operation into two parts (for example, two halves), then
12 sending that one half part to each to two connected available
13 slave personal computers PC 1 (or microprocessor 40), as shown
14 one level down as S_{21} and S_{22} .

15 Figure 16B shows that slave personal computer PC 1 (or
16 microprocessor 30) located at S_{21} has temporarily adopted the
17 same functional role as a master to repeat the same
18 subdivision of the given operation. Therefore, the given
19 operation already divided in half is further subdivided into
20 quarters (for example) by S_{21} , which then sends one quarter to
21 each of two additional available personal computers PC 1 (or
22 microprocessors 40) located at S_{31} and S_{32} .

23 Figure 16C shows personal computers PC 1 (or
24 microprocessors 40) at S_{31} and S_{32} sending operation results
25 back to S_{21} , instead of repeating again the subdivision
26 process. That action by S_{31} and S_{32} can be dictated by pre-
27 established program criteria, such as automatically defaulting

1 to operational processing at the S_1 level after two
2 subdivision processes, so that the operation would be
3 processed in parallel by four slave personal computers PC 1
4 (or microprocessors 40). Alternately, as another example, the
5 criteria can be a user preference command over-riding an
6 otherwise automatic default to level three processing.

7 Similarly, in Figure 16A above, the personal computer PC
8 1 (or microprocessor 40) acting as master M_1 also initiates
9 the parallel processing operation (or, alternatively, a multi-
10 tasking operation) on the basis of a preset program parameters
11 through software, hardware, or firmware or other means,
12 parameter examples again being automatic default or user
13 preference.

14 Like Figure 16C, Figure 16D shows operation results
15 being passed back to the next higher level, this time from
16 slave personal computers (or microprocessors 40) S_{21} and S_{22} to
17 master M_1 .

18 Figure 16G shows master personal computer (or
19 microprocessor 30) M_1 offloading the entire parallel
20 processing operation to an available slave personal computer
21 (or microprocessor 40) PC 1 that temporarily functions as S_1
22 in the place of M_1 on the first level for the duration of the
23 operation, the first step of which is shown in Figure 16H.

24 Figure 16I shows a personal computer (or microprocessor
25 40) PC 1 that is executing a command to function in the role
26 of S_{21} for a given operation but has become unavailable or was
27 unavailable initially (due, for example, to interruption for

1 other higher, priority use or malfunction), when results of
2 the given operation from a lower parallel processing level are
3 passed to S_{21} . S_{21} simply offloads those results to another
4 personal computer PC 1 (or microprocessor 30 or 40) that is
5 available which becomes S_{21} . and takes over the role of S_{21} in
6 the given operation.

7 As shown in Figure 16J, S_{21} then completes the parallel
8 processing operation by passing the operation results to M_1 .

9 The offloading capability of functional roles of master
10 and slave personal computers PC 1 (and microprocessors 30 and
11 40) from unavailable to available PC 1, 30 and 40 as shown in
12 Figures 16G-16J can also be used in previous figures in this
13 application.

14 Figure 16E shows the multi-processing network topology
15 in a larger scale embodiment, including all personal computers
16 PC 1 (or microprocessors 30 or 40) that are participating in a
17 given operation, including one at level one; two at level two;
18 four at level three; and eight at level four. The network
19 topology is completely scalar in that any practical number of
20 additional processing levels or personal computers PC 1 (or
21 microprocessors 30 or 40) can be added to those shown (and
22 topologies limited to just two levels are also possible).

23 More specifically, Figure 16E shows the distribution of
24 a parallel processing (or multi-tasking) operation as routed
25 through a four level virtual network, beginning at M_1 .
26 "Virtual" as used here means temporary, since in the next
27 parallel operation originating at M_1 it might be the case that

1 many of the personal computers PC 1 (or microprocessors 30 or
2 40) that had been available for a previous operation would not
3 still be available for the next operation.

4 Figure 16F shows the processing slave personal computers
5 PC 1 (or microprocessors 40) at the fourth level, where S_{41}
6 through S_{48} process the operation to produce results which are
7 then routed back through the virtual network to M_1 . Figure
8 16F shows an inverted view of Figure 16E.

9 In the routing of operation results shown in Figure 16F,
10 each slave personal computer PC 1 (or microprocessor 40) has
11 the capability to either simply pass through those results or,
12 alternatively, to consolidate those results sent from the
13 personal computers PC 1 (or microprocessors 40) at a lower
14 level.

15 Such consolidation could eliminate duplicative data from
16 a search or other duplicative results and also serve to buffer
17 the originating master M_1 from overloading caused by many sets
18 of results arriving in an uncoordinated fashion from what
19 might be a large number of slave personal computers PC 1 (or
20 microprocessors 40). Such a consolidation role for personal
21 computers PC 1 (or microprocessors 40) would substantially
22 reduce or eliminate the excessive custom pre-planning and
23 synchronization problems of the conventional Figure 9 network
24 topology discussed above.

25 Figure 16K shows examples of the extremely complicated
26 network structures that can result from a given operation in
27 which the complexity of data involved is not uniform. In this

1 case, pre-set program splitting criteria can be employed that
2 balances the processing load of each slave personal computer
3 PC 1 (or microprocessor 40). With this approach, the
4 difficult portions of a given operation can automatically draw
5 greater resources in the form of additional splitting of that
6 difficult portion of the problem, so that additional levels of
7 parallel processing slave personal computers PC 1 (or
8 microprocessors 40) can be brought into the virtual network to
9 process the operation.

10 Figures 16L and 16M show examples of other possible
11 subdivision parallel processing methods, such as routing to
12 three slave personal computers PC 1 (or microprocessors 40) at
13 the next level down, as shown in Figure 16L, or routing to
14 four slave personal computers PC 1 (or microprocessors 40), as
15 shown in Figure 16M. Routing to any practical number of slave
16 personal computers PC 1 (or microprocessors 40) between levels
17 can be done.

18 Such routing splits can also vary between levels or even
19 within the same level, as shown in Figure 16N; such variations
20 can result from pre-set program criteria that balance
21 operation loads, like those shown previously in Figure 16K.
22 The means for subdividing problems for parallel processing can
23 also vary, within a range of methods in the computer and
24 mathematical art.

25 Figure 16O shows slave personal computer PC 1 (or
26 microprocessor 40) S_{41} sending operation results to a higher
27 level S_{31} , which can then function as a router, passing through

unaltered the results back down to the original level to personal computer PC 1 (or microprocessor 40) S_{42} , as shown in Figure 16P. Figure 16Q demonstrates the capability for any two pair of slave personal computers PC 1 (or microprocessors 40) like S_{41} and S_{42} to communicate directly between each other, such as wirelessly as shown. Figures 16O-16Q shown the same subsection of the network topology shown in Figure 16F (the left uppermost portion).

A higher level personal computer PC 1 (or microprocessor 30 or 40) such as S_{31} can process results as well as route them, as shown in Figure 16V, in which S_{31} receives results from S_{41} and S_{42} at a lower processing level and then processes that data before sending its processing results to a higher level to S_{21} , as shown in Figure 16W.

Together, Figures 16V-16W and 16O-16Q show the capability of any personal computer PC 1 (or microprocessor 30 or 40) of the Figure 16F (and 16E) network structural and functional invention to communicate with any other personal computer PC 1 (or microprocessor 30 or 40) participating in a given parallel processing (or multi-tasking) operation. That communication can take the form of simple pass-through of unmodified results or of modification of those results by processing at any level.

Figures 16X-16Z show the applicant's new hierarchical network structure and function applied to the design of a personal computer PC 1, as discussed previously in Figures 10A and 10B. Figure 10X shows the simplest general design, with a

1 master M_1 microprocessor 30 and two slave S_{21} and S_{22}
2 microprocessors 40. Figure 16Y shows the same network
3 structure with an additional level of slave microprocessors
4 40, S_{31} through S_{34} , while Figure 16Z shows the same network
5 structure as Figure 16Y with an additional level of slave
6 microprocessors 40, S_{41} through S_{48} . As shown, this network
7 structure is completely scalar, including any practical number
8 of slave microprocessors 40 on any practical number of
9 processing levels.

10 Figure 16AA shows a useful embodiment in which each
11 microprocessor 30 and 40 has its own random access memory.
12 The design can also incorporate (or substitute) conventional
13 shared memory (i.e. memory used by all, or some, of the
14 microprocessors 30 or 40 of the PC 1).

15 Figures 16R-16T are parallel to Figures 16X-16Z above,
16 but show microprocessor 90 architecture rather than PC 1
17 architecture. Figure 16U is like Figure 16AA, also except for
18 showing microprocessor 90 architecture.

19 Figures 16R-16U show a different and improved basic chip
20 architecture from than currently used to implement a
21 superscalar approach in microprocessors to execute multiple
22 instructions during each clock cycle. The Figures 16R-16U
23 architecture is much simpler and, by integrating memory with
24 microprocessor, reduces memory bottlenecks. Figures 16X-16Z
25 and 16AA, by using the same architecture for PC 1 networks,
26 import the same advantage of improved chip superscalar
27 performance to parallel processing in PC 1 networks.

1 Figure 17A shows a firewall 50 performing its
2 conventional function of keeping out intruders such as hackers
3 from the Internet 3. Figure 17B shows that, since Internet
4 users can, as enabled by the applicant's network structure
5 invention, use one or more of the slave microprocessors 40 of
6 another's PC 1 for parallel processing (or multi-tasking), the
7 firewall 50 has a dual function in also protecting Internet
8 use (or other shared use on a network) from unauthorized
9 surveillance or intervention by a PC 1 owner/user. To
10 maintain the privacy necessary to operate such a cooperatively
11 shared network arrangement, unauthorized surveillance or
12 intervention must be carefully prevented.

13 Figure 17C therefore shows master M personal computer PC
14 1 using the slave microprocessor 40 of a different personal
15 computer, PC 1', which is available for Internet (or other
16 net) shared use, while firewall 50' blocks unauthorized access
17 by PC 1 (although PC 1' owner/user can always interrupt a
18 shared operation and take back control and use of slave S'
19 microprocessor 40).

20 Figure 17D shows a figure similar to Figure 17C, but
21 showing a microprocessor 90 with a slave microprocessor 94
22 being used by Internet users (or other net), so that firewall
23 50 serves both to deny access by master M microprocessor 93 to
24 an Internet parallel processing (or multi-tasking) operation
25 on slave S microprocessor 94 and to deny access to master M
26 microprocessor 93 by Internet (or other net) users of slave S
27 microprocessor 94.

1 Figures 18A-18D show designs for a virtual quantum
2 computer or computers. Figure 18A shows personal computer PC
3 1 with a software program simulating a "qubit" for a quantum
4 computer or computers. Figure 18B shows a personal computer
5 PC 1 with a digital signal processor (DSP) connected to a
6 hardware analog device simulating a qubit, with the PC 1
7 monitoring the qubit through the DSP; this arrangement would
8 allow the option of simultaneous use of the PC 1 through
9 multi-tasking for both digital and quantum computing.

10 Figure 18C is like Figure 16A, but incorporating a
11 virtual qubit in PC 1, so that a virtual quantum computer can
12 have any network architecture like those shown in Figures 16A-
13 16Z and 16AA, as well as other figures of this application.

14 As shown in Figure 18D, for example, a virtual qubits
15 (VC) network can provide complete interconnectivity, like
16 Figure 13. Virtual qubits VC like those described in Figures
17 18A & 18B can be added to or substituted for microprocessors
18 30 and 40 in prior figures of this application. As shown in
19 those prior applications, the number of qubits is limited only
20 to whatever is practical at any given time; in terms of
21 development that means as few as a single qubit in one or more
22 networked personal computers PC 1 to begin, but the number of
23 qubits can become potentially extremely large, as indicated in
24 previous figures.

25 Like personal computers located in the home or office,
26 personal computers PC 1 in automobiles (including other
27 transportation vehicles or other conveyances) are in actual

1 use only a very small percentage of the time, with the average
2 dormant period of non-use totaling as much as 90 percent or
3 more. Personal computers PC 1 are now being added to some
4 automobiles and will likely soon become standard equipment.
5 In addition, automobiles already have a very large number of
6 computers onboard in the form of specialized microprocessors
7 which are likely to become general parallel processors in
8 future designs, as discussed earlier in this application.

9 Automobiles therefore form a potentially large and
10 otherwise unused resource for massive parallel processing
11 through the Internet 3 and other networks, as described in
12 earlier figures. However, when idle and thus generally
13 available for network use, automobiles lack their usual power
14 source, the engine, which of course is then off, since it is
15 too large to efficiently provide electrical power to onboard
16 computers. The car engine have a controller (hardware,
17 software or firmware or combination in the PC 1, for example)
18 to automatically start in order to recharge the car battery
19 when the battery is low (and before the battery is too low to
20 start the engine), but the engine additionally needs to be
21 controlled not to expend all available fuel automatically.

22 Two solutions, not mutually exclusive, to alleviate (but
23 not solve) the problem are adding an additional car battery
24 for network use (at least primarily) or using a single battery
25 but adding a controller in the PC 1 for example that prevents
26 the existing battery from being discharged to a level below
27 that which is needed to start the automobile.

1 In addition, one or more solar power generating cells or
2 cell arrays can be incorporated in an automobile's outer
3 surface, with generally the most effective placement being on
4 a portion of the upper horizontal surface, such as a portion
5 of the roof, hood, or trunk. For charging the automobile
6 battery when sunlight is not available, such as at night or in
7 a garage, a focused or focusable light source can provide
8 external power to the solar panel.

9 Alternately, a connection device such as a plug for an
10 external electrical power source can be installed on or near
11 the outer surface of the automobile. In addition, or
12 independently, a connection device for an optical fiber (or
13 other wired) external connection to the Internet 3 or other
14 net. Alternately, a wireless receiver located near where the
15 automobile is parked, such as in a garage, can provide
16 connection from the automobile's personal computers PC 1 to a
17 network (and the Internet 3) in a home or business. This
18 application encompasses all new apparatus and methods required
19 to operate the above described network computer system or
20 systems, including any associated computer or network
21 hardware, software, or firmware (or other component), both
22 apparatus and methods. Specifically included, but not limited
23 to, are (in their present or future forms, equivalents, or
24 successors): all enabling PC and network software and firmware
25 operating systems, user interfaces and application programs;
26 all enabling PC and network hardware design and system
27 architecture, including all PC and other computers, network

1 computers such as servers, microprocessors, nodes, gateways,
2 bridges, routers, switches, and all other components; all
3 enabling financial and legal ytransactions, arrangements and
4 entities for network providers, PC users, and/or others,
5 including purchase and sale of any items or services on the
6 network or any other interactions or transactions between any
7 such buyers and sellers; and all services by third parties,
8 including to select, procure, set up, implement, integrate,
9 operate and perform maintenance, for any or all parts of the
10 foregoing for PC users, network providers, and/or others.

11 The combinations of the many elements the applicant's
12 invention introduced in the preceding figures are shown
13 because those embodiments are considered to be at least among
14 the most useful possible, but many other useful combination
15 embodiments are not shown simply because of the impossibility
16 of showing them all while maintaining a reasonable brevity in
17 an unavoidably long description caused by the inherently
18 highly interconnected nature of the inventions shown herein,
19 which can operate all as part of one system or independently.

20 The forgoing embodiments meet the objectives of this
21 invention as stated above. However, it will be clearly
22 understood by those skilled in the art that the foregoing
23 description has been made in terms of the preferred
24 embodiments and that various changes and modifications may be
25 made without departing from the scope of the present
26 invention, which is to be defined by the appended claims.

Figure 20A is like Figure 16Y, but also shows a slave microprocessor 40 functioning as S_1 , the function of master having been temporarily or permanently offloaded by M_1 microprocessor 30. In addition, Figure 20A shows the processing level of slave microprocessors 40, S_{31} through S_{34} , each with a separate output link to a digital signal processor 89, the transmission linkages shown as 111, 112, 113, and 114. The DSP is connected to wired 99 link (preferably fiber optic) to the Internet (or other net), although non-fiber optic can be used (and probably would not require a DSP 89).

Figure 20B is like Figure 16S, but with the same new additions as Figure 20A. Figure 20B shows additionally two more level of parallel processing by personal computer on a chip-type microprocessors 90, consisting of a second level with microprocessors 90_{21} through 90_{24} and a third level with microprocessors 90_{31} through 90_{316} consisting of 16 microprocessors 90. Each of the three processing levels is separated by an intermediate direct connection to the Internet 3 (or other net) and by four output lines from the higher processing level. Microprocessors 90_{21} through 90_{24} are shown receiving respectively the outputs 111 through 114 from slave microprocessors 94, S_{31} through S_{34} . (Note that microprocessor 90_1 is shown in detail including all slave microprocessors 94, while other PC microprocessors at the second and third levels do not.)

Figure 20B shows that between each processing level the output links from every PC microprocessor 90 can be transmitted from slave microprocessors 94 directly to PC microprocessors 90 below, such as from PC microprocessor 90_{21} to PC microprocessors 90_{31} through 90_{34} , via the Internet 3 or other net. Each of the transmission links from slave processing microprocessors 94, S_{31} through S_{34} , shown as 111, 112, 113, and 114 for PC microprocessor 90_1 , can be transmitted on a different channel on a fiber optic direct connection to the PC microprocessor chip 90 through the digital signal processor 89, of which there may be one or more.

IN THE CLAIMS:

1. A system for a network of computers, including personal computers, comprising:

at least three personal computers;

one said personal computer functioning as a master in a parallel processing or multi-processing operation involving at least two other said personal computers functioning as slaves to said master;

hardware or software or firmware means for said master personal computer to subdivide said operation into two parts and to send said parts to said slaves for processing by said slaves;

hardware or software or firmware means for said at least two slave personal computers to process said operation and send results back to said master when the operation is completed.

2. The system of claim 1, wherein said system is scalar in that said system imposes no limit to the number of said personal computers.

3. The system of claim 2, wherein said system includes at least 1024 said personal computers.

4. The system of claim 1, wherein said system is scalar in that said system imposes no limit to the number of said personal computers participating in a single shared computer processing operation.

5. The system of claim 4, wherein said system includes at least 256 said personal computers.

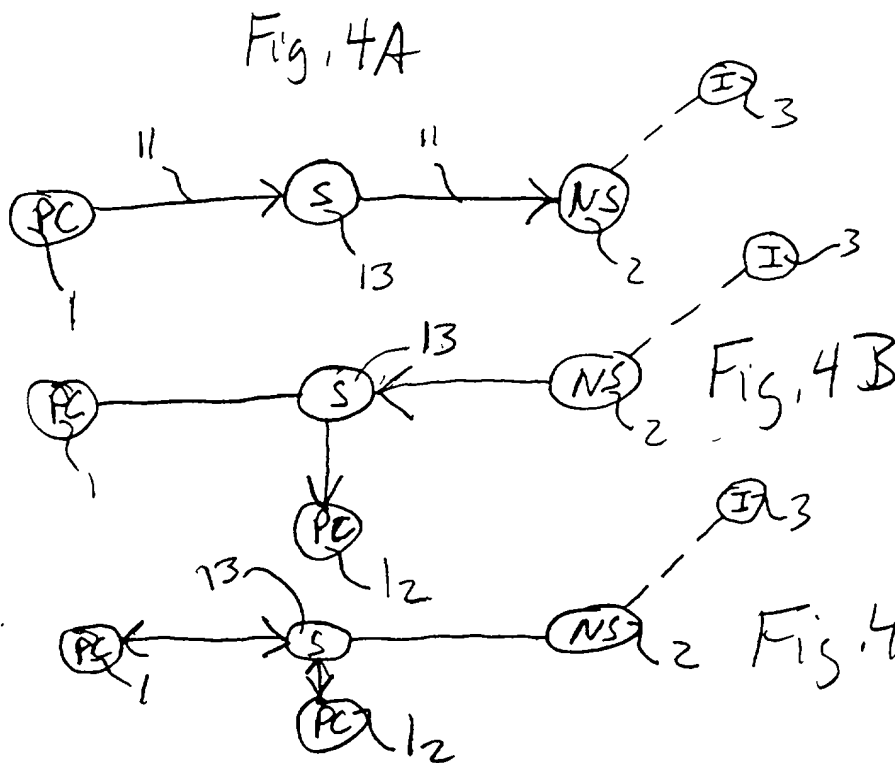
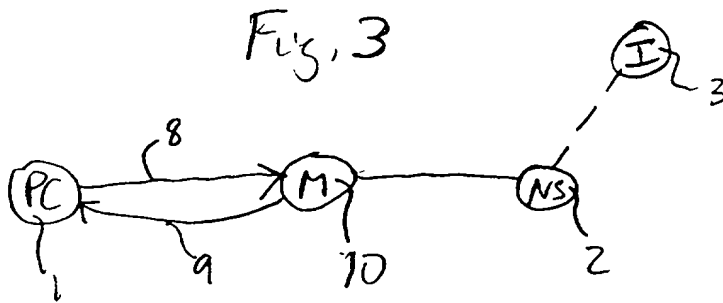
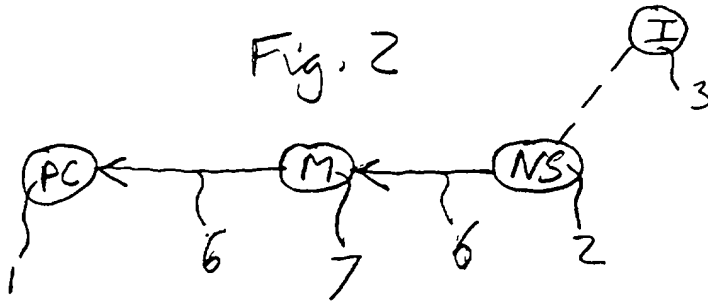
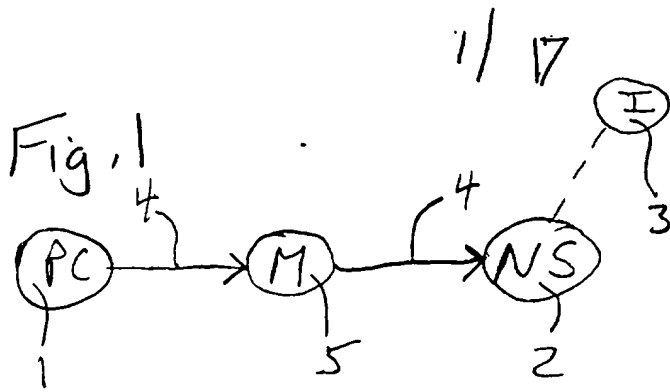
6. The system of claim 1, wherein said network is connected to the Internet and its equivalents and successors, so that said personal computers include at least a million personal computers.

7. The system of claim 1, wherein said network is connected to the World Wide Web and its successors.

8. The system of claim 1, wherein said network includes at least one network server that participates in said shared computer processing.

Abstract of the Disclosure

This invention generally relates to one or more computer networks having computers like personal computers or network servers with microprocessors linked by broadband transmission means and having hardware, software, firmware, and other means such that at least one parallel processing operation occurs that involve at least two computers in the network. More particularly, this invention relates to one or more large networks composed of smaller networks and large numbers of computers connected, like the Internet, wherein more than one separate parallel processing operation involving more than one different set of computers occurs simultaneously and wherein ongoing processing linkages can be established between virtually any microprocessors of separate computers connected to the network. Still more particularly, this invention relates to business arrangements enabling the shared use of network microprocessors for parallel and other processing, wherein personal computer owners provide microprocessor processing power to a network, preferably for parallel processing, in exchange for network linkage to other personal and other computers supplied by network providers, including linkage to other microprocessors for parallel or other processing; the basis of the exchange between owners and providers being whatever terms to which the parties agree, subject to governing laws, regulations, or rules, including payment from either party to the other based on periodic measurement of net use or provision of processing power.



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Fig. 5A

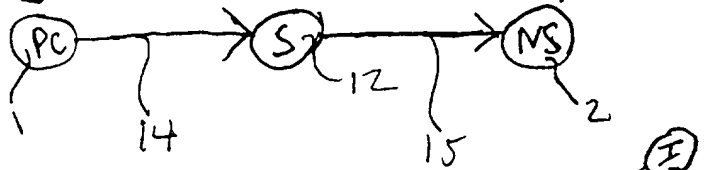


Fig. 5B

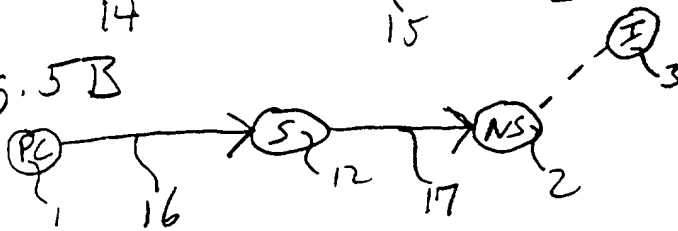


Fig. 6

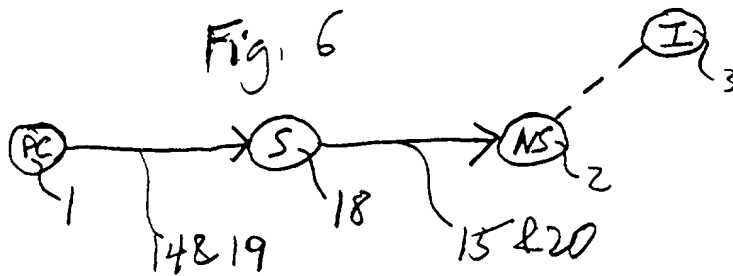


Fig. 7

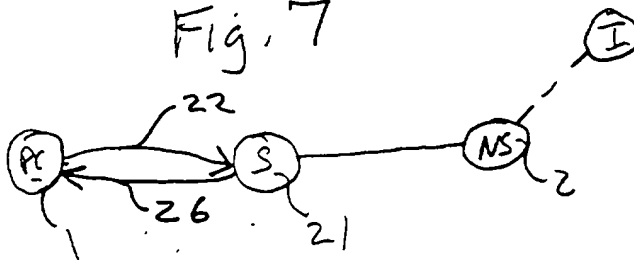
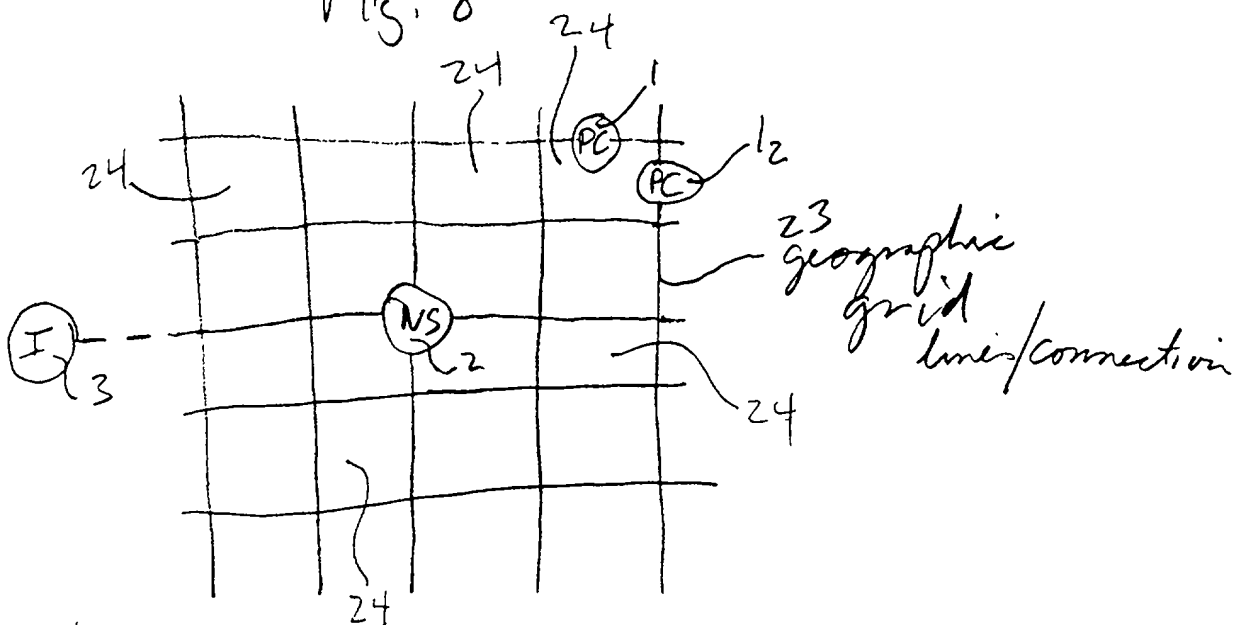
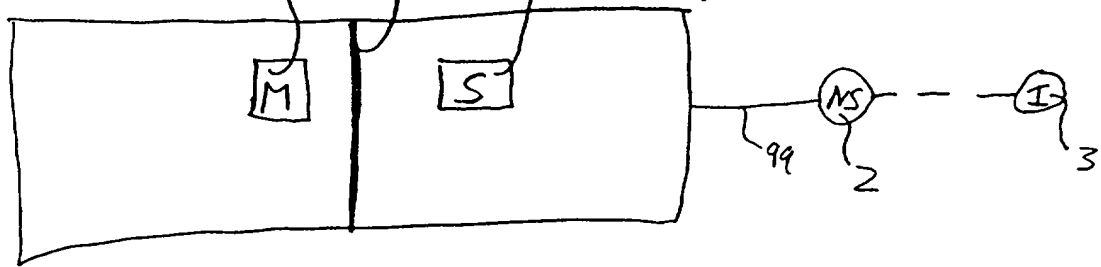


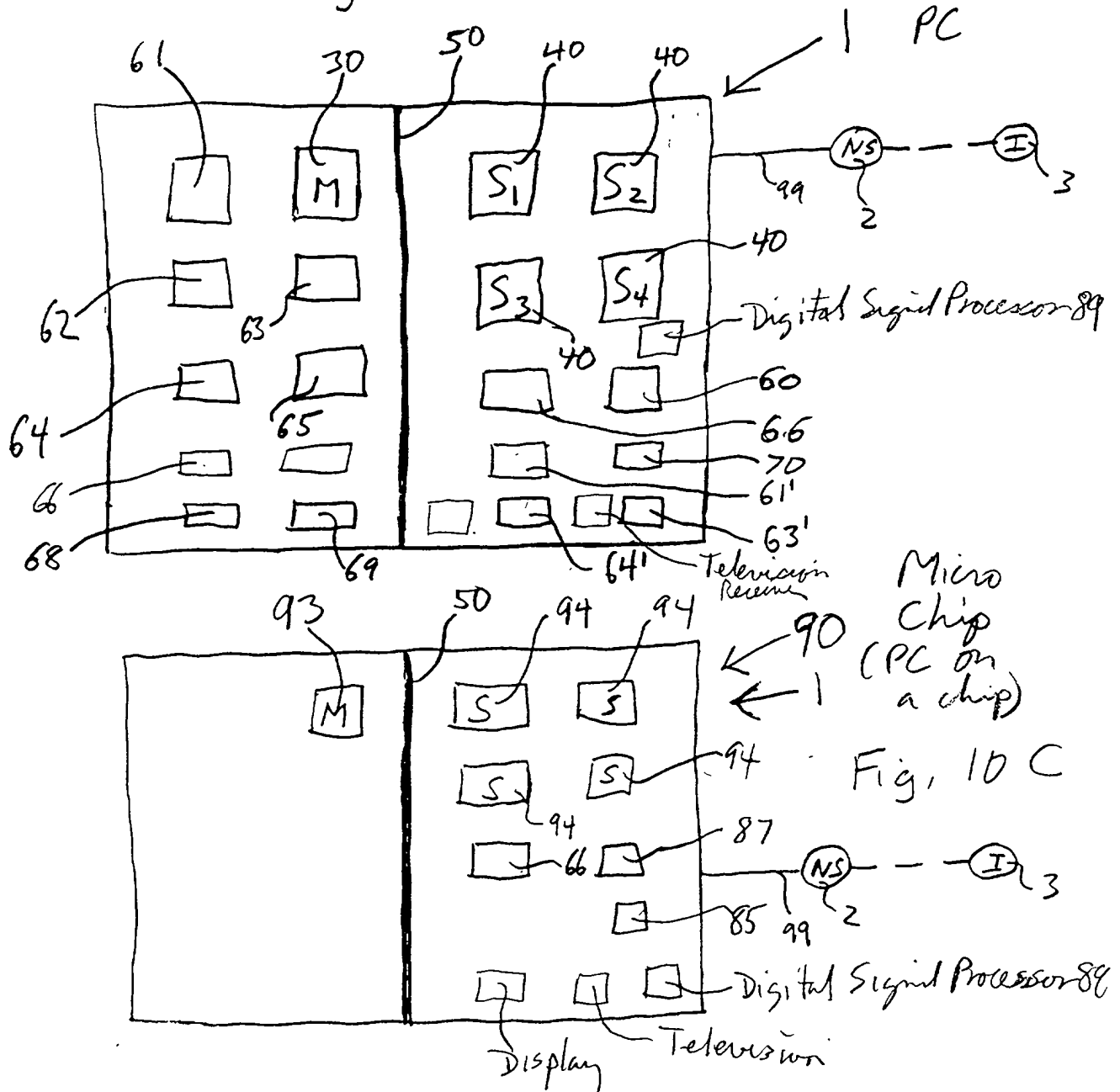
Fig. 8



40



PC



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Fig. 9

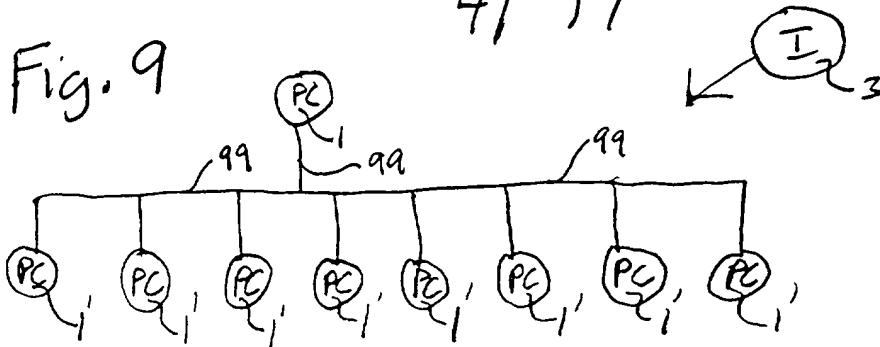


Fig. 10 D

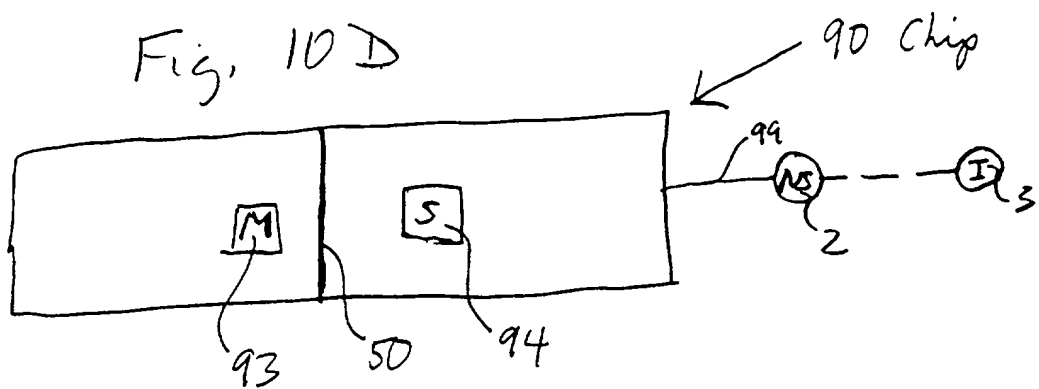


Fig. 11

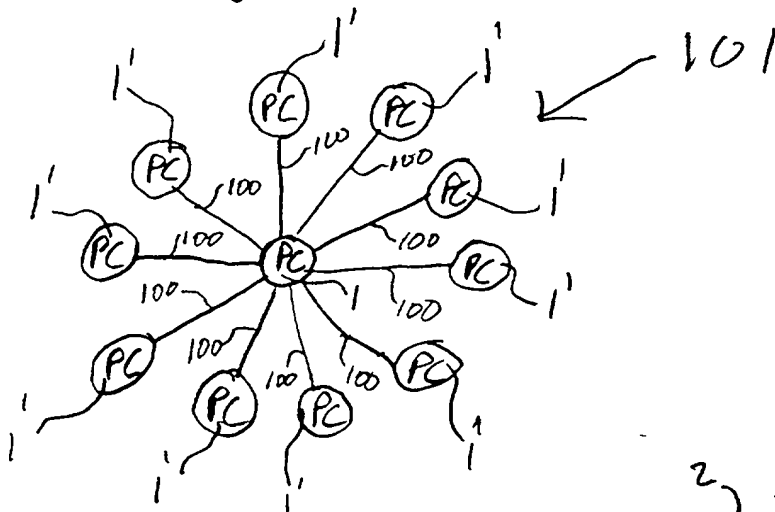
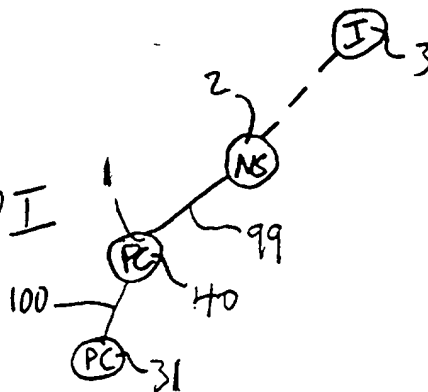


Fig. 10 I



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Fig. 10E

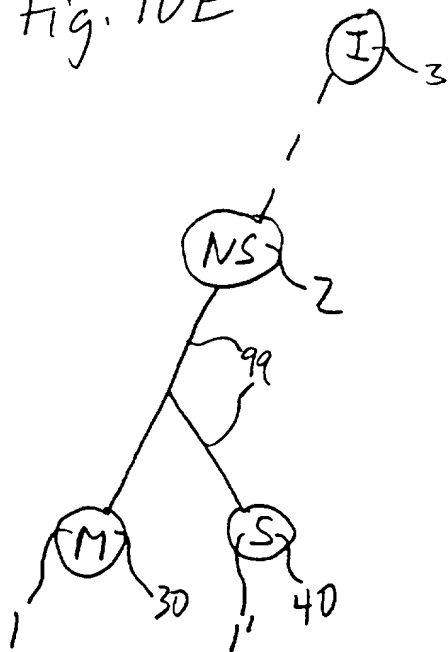


Fig. 10F

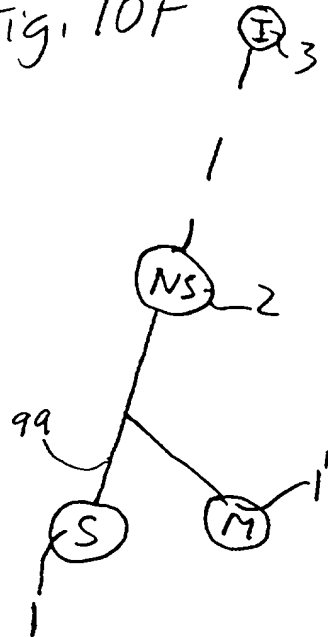


Fig. 10G

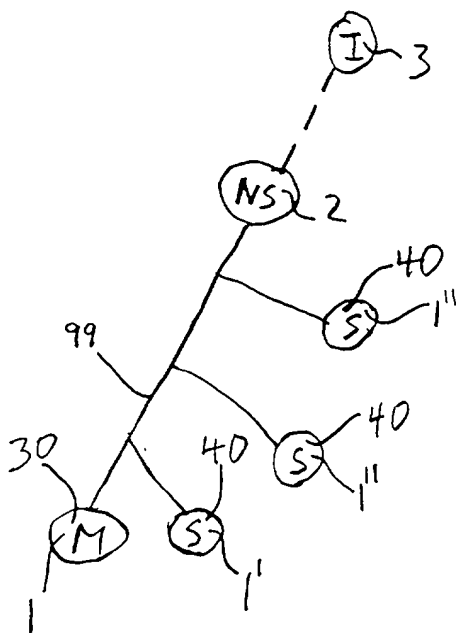
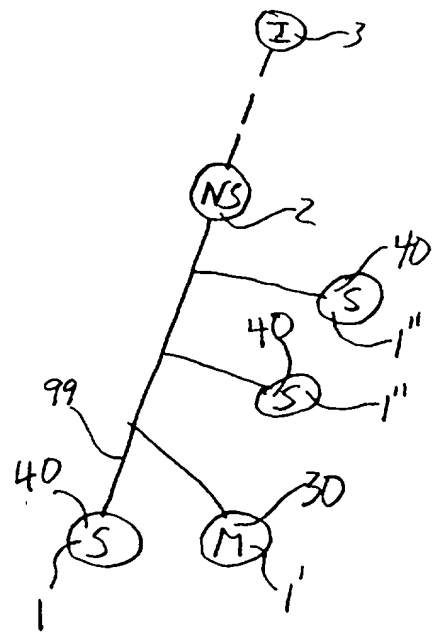


Fig. 10H



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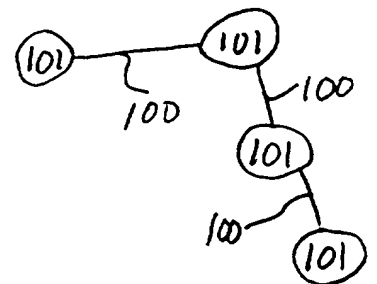
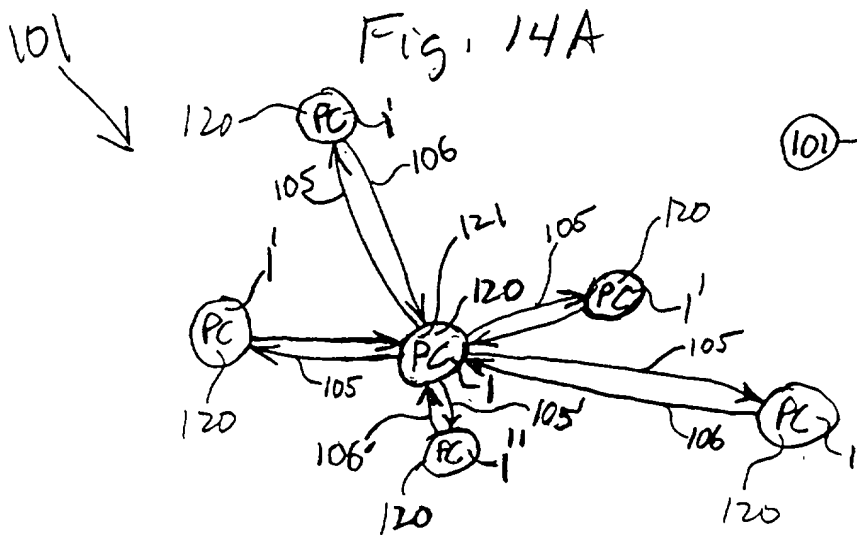
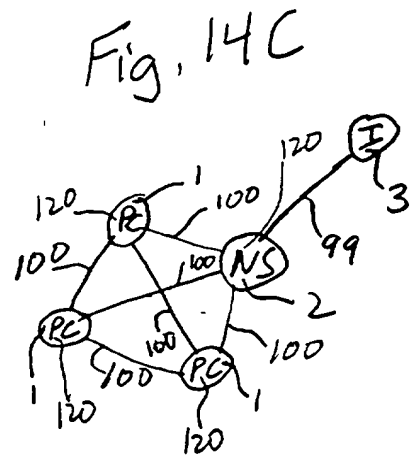
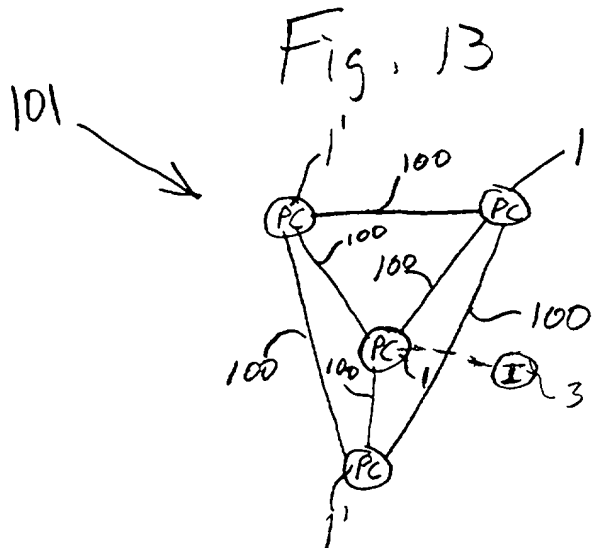
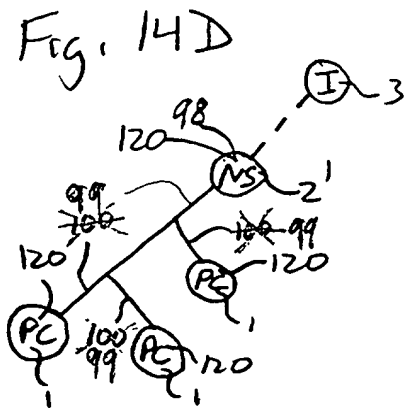
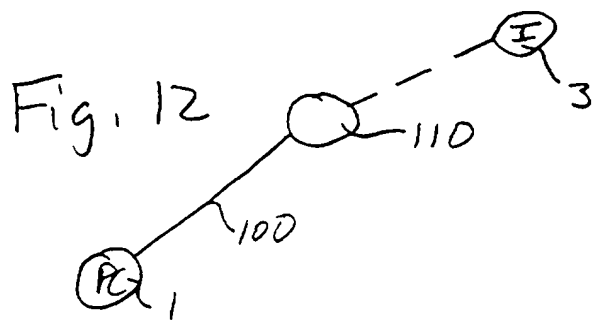
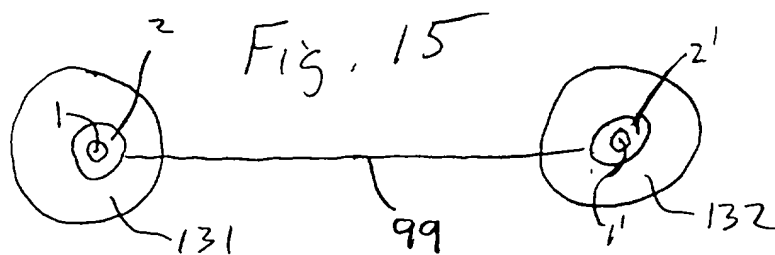


Fig. 14B



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Fig. 10K

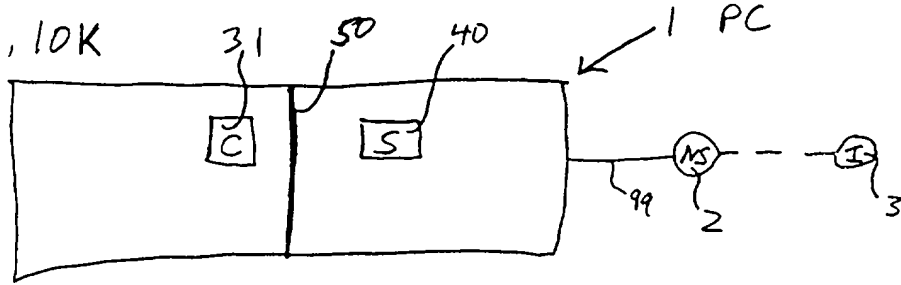


Fig. 10J

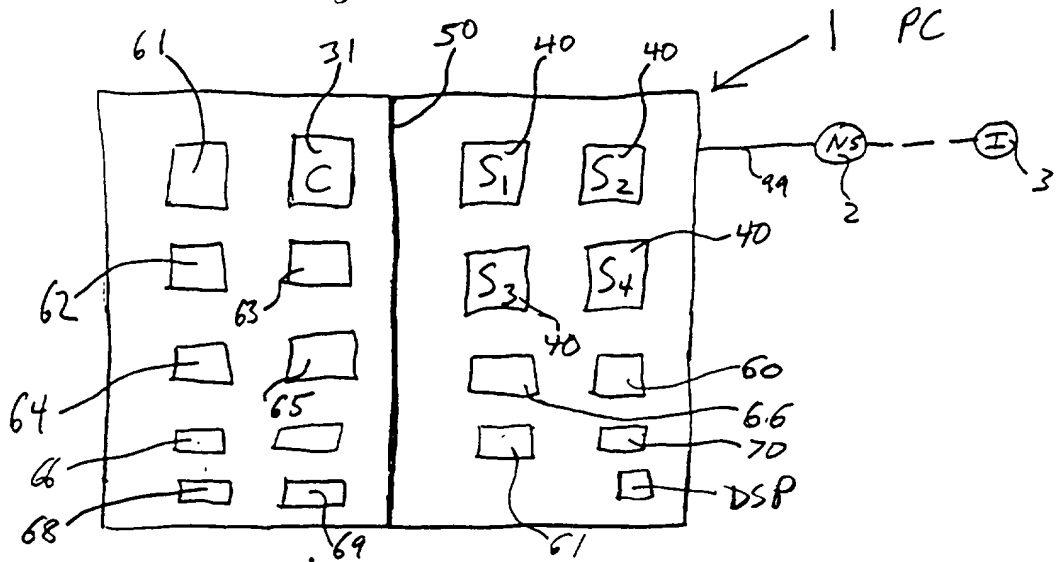


Fig. 10L

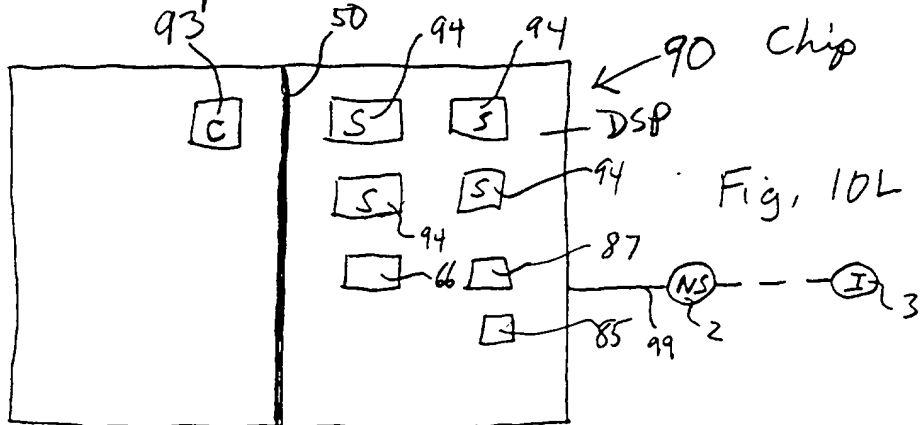
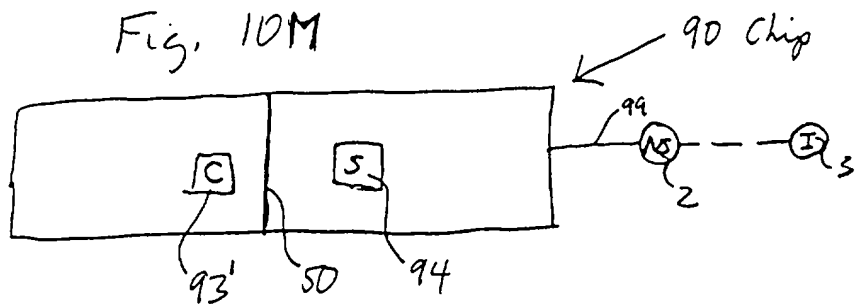


Fig. 10M



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Fig. 10"O"

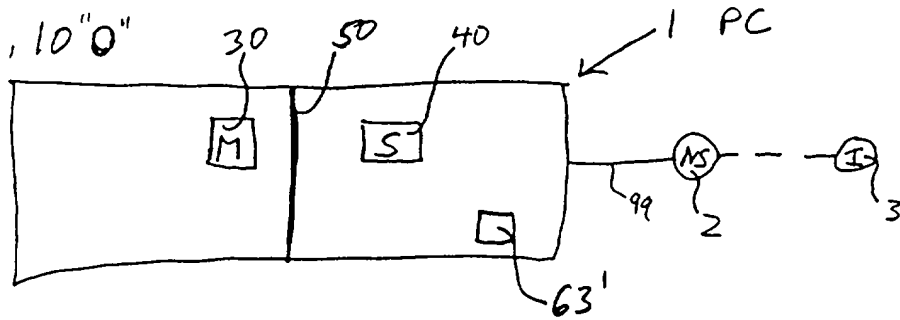


Fig. 10N

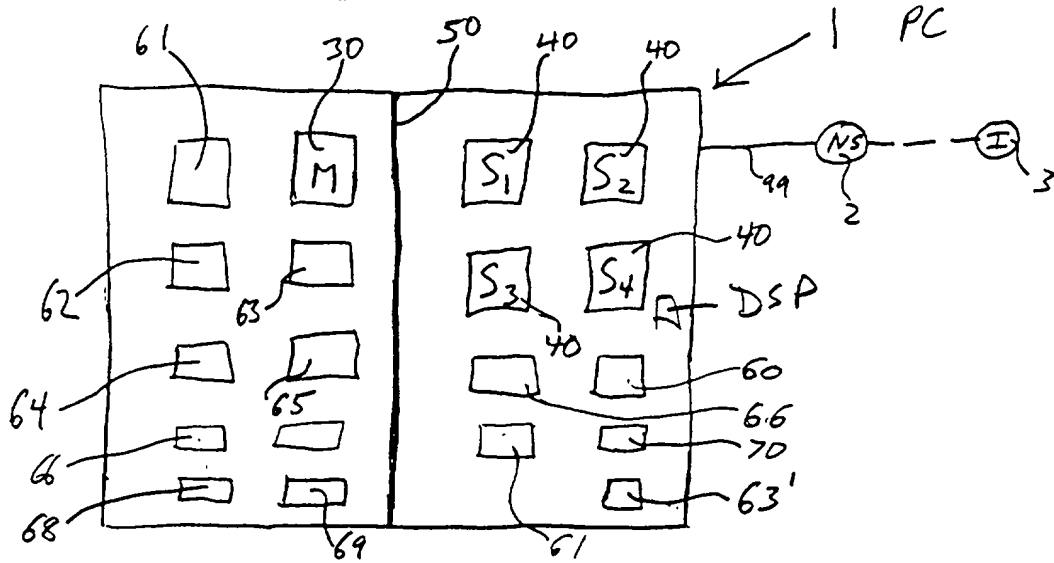


Fig. 10 P

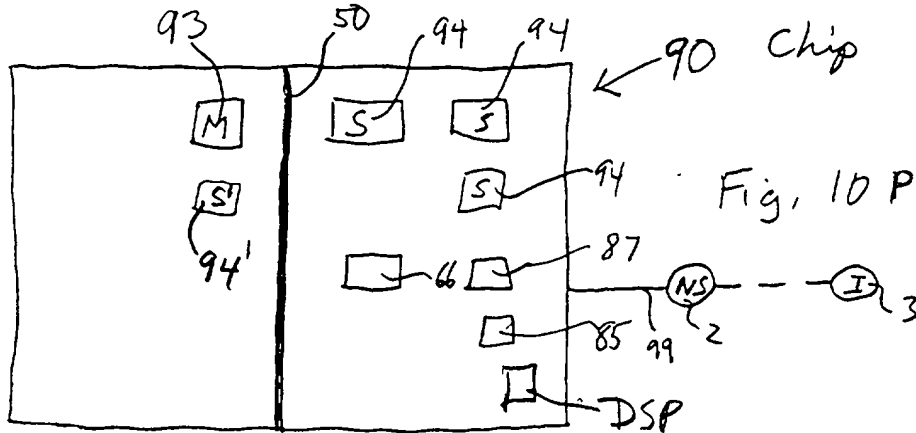
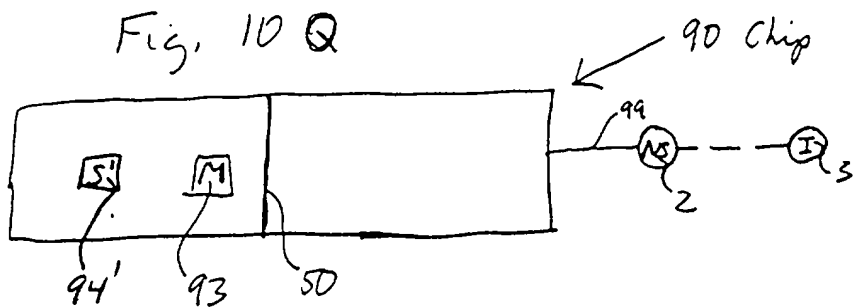
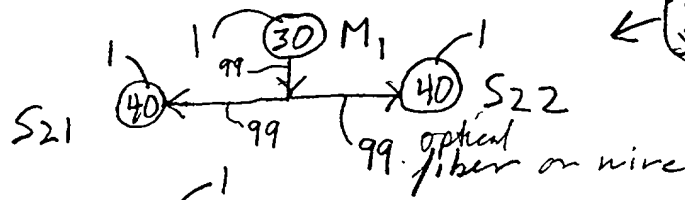


Fig. 10 Q



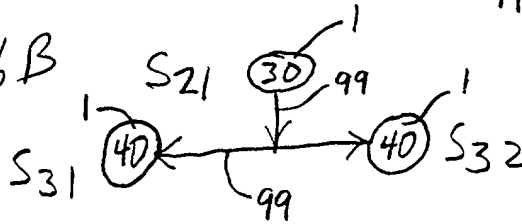
9/17

Fig. 16A



← (I) (Part of Internet or Intranet or other net)

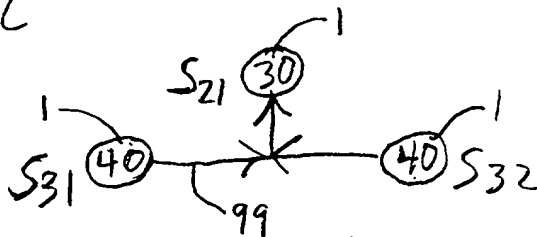
Fig. 16B



← (I) 3

Figs 16A-Q & 16V-AA:

Fig. 16C



← (I) 3

1-(30) indicates either master PC 1 or master microprocessor 30 chip within a PC 1.

Like wise, 1-(40) indicates either a slave PC 1 or a slave microprocessor 40 chip within a PC 1.

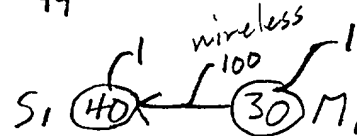
Fig. 16D



← (I) 3

Either microprocessor 30 or microprocessor 40 can be a microprocessor 90, a PC 1 or a microder

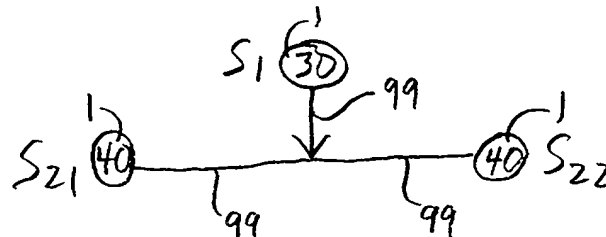
Fig. 16G



← (I) 3

Note 100: mix of 100 & 99

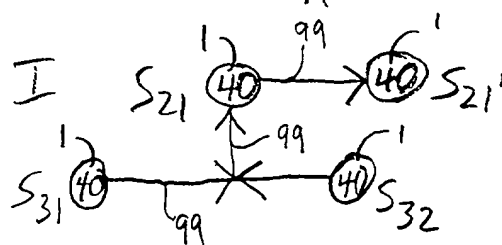
Fig. 16H



← (I) 3

Master PC offloads operation to Slave PC's which functions as on

Fig. 16I



← (I) 3

Unavailable S21 offloads results of S31 & S32 to S21' which takes over

Fig. 16J



← (I) 3

Like Fig. 16D S21' replaces S21

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Fig. 16 E

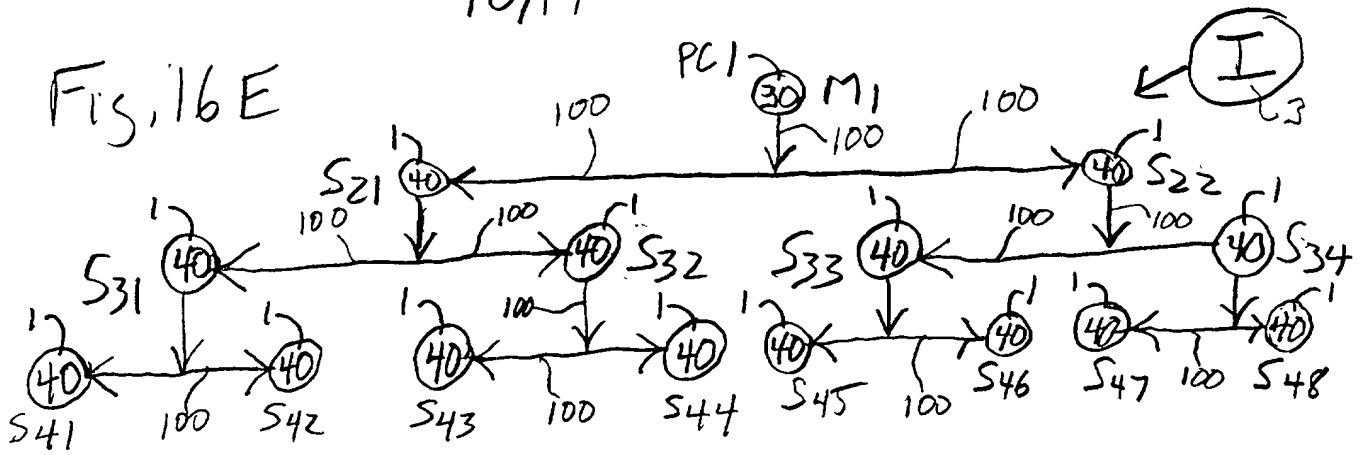


Fig. 16 F

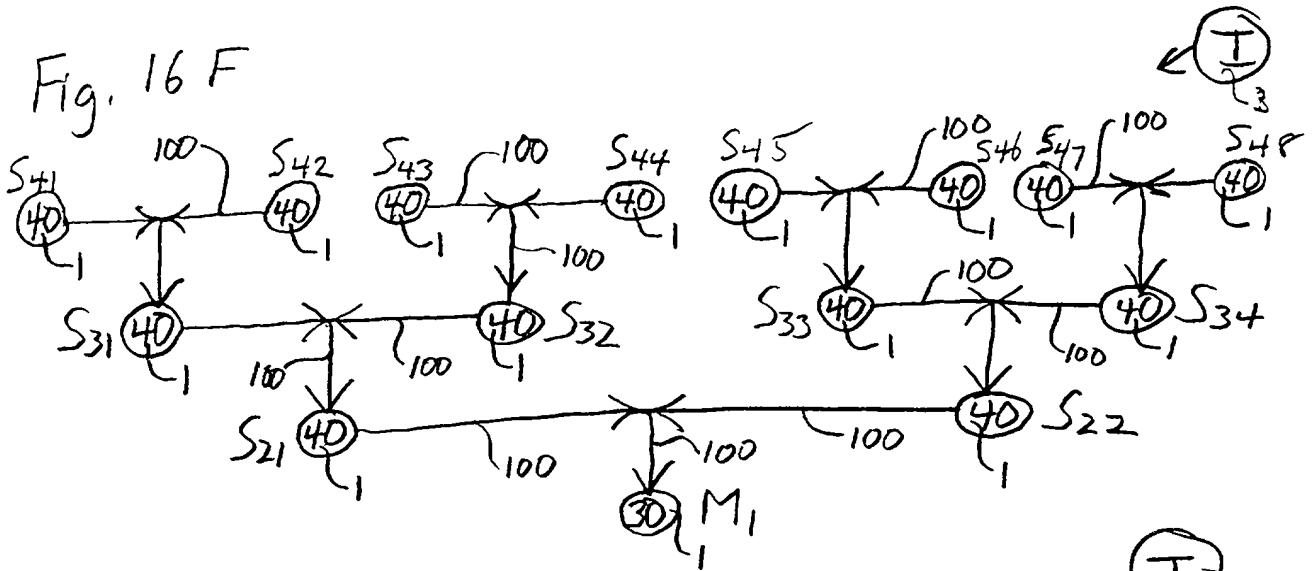
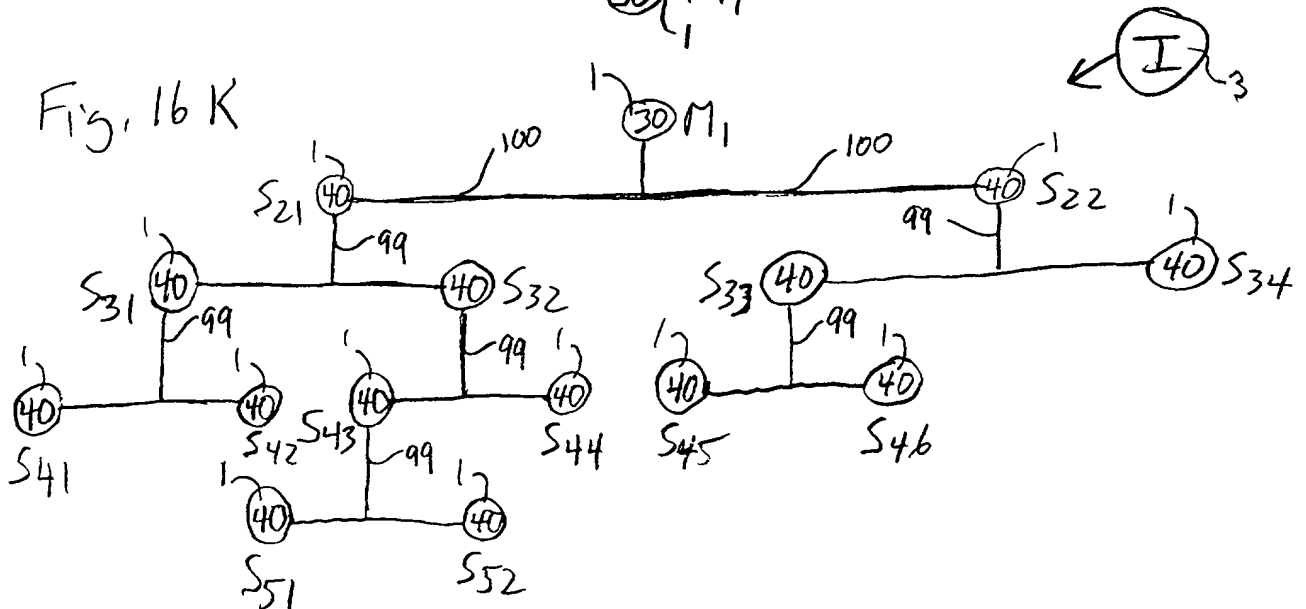


Fig. 16 K



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Fig. 16L

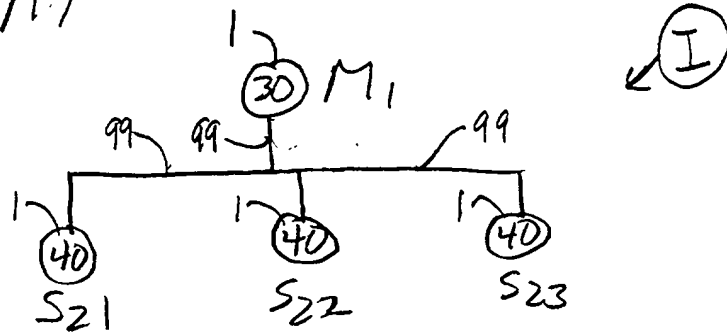


Fig. 16M

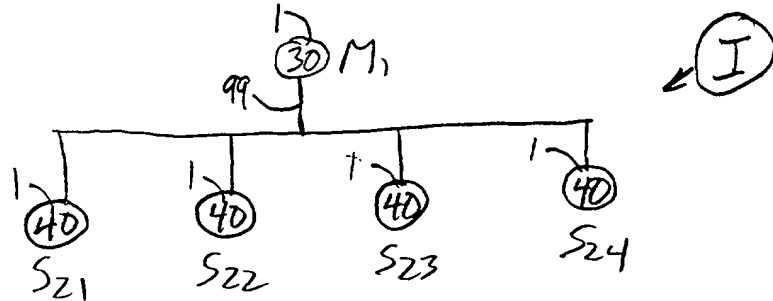


Fig. 16N

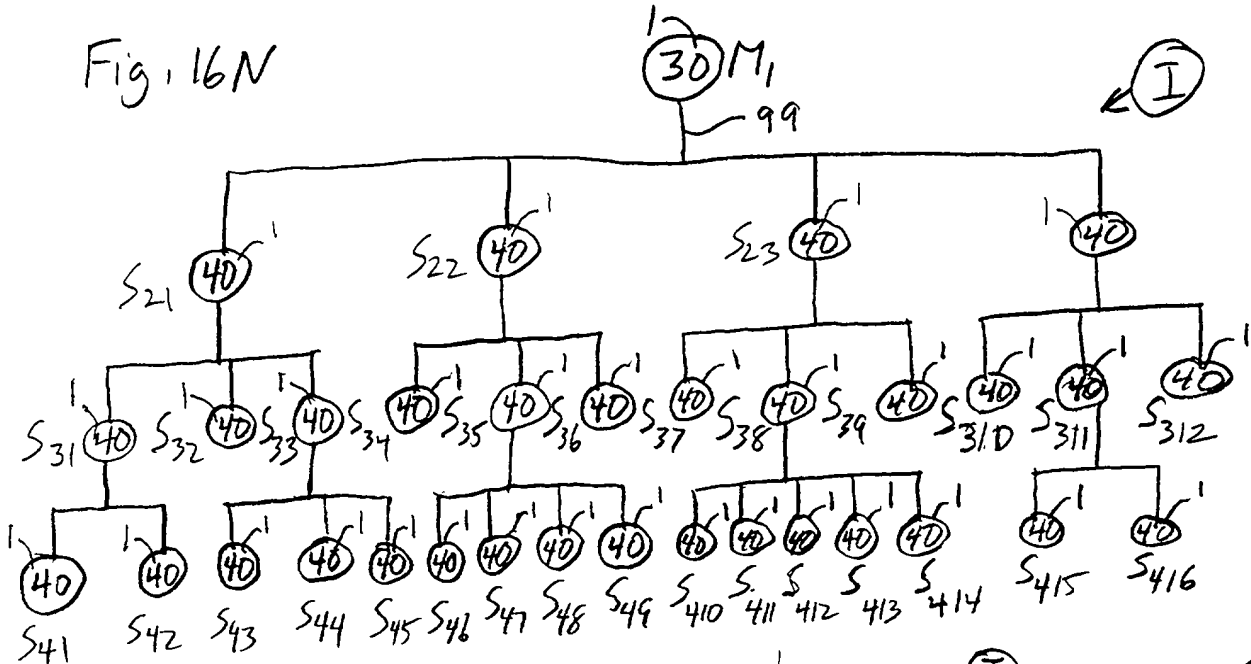


Fig. 16O

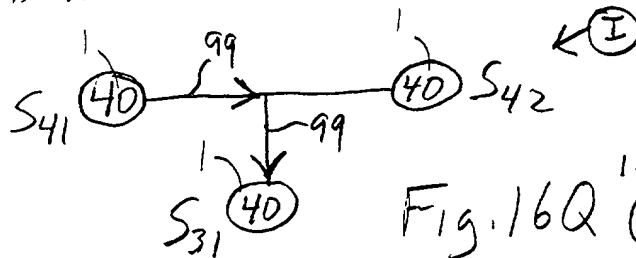


Fig. 16Q

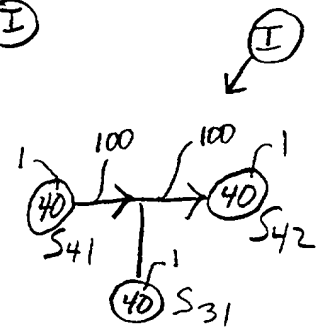
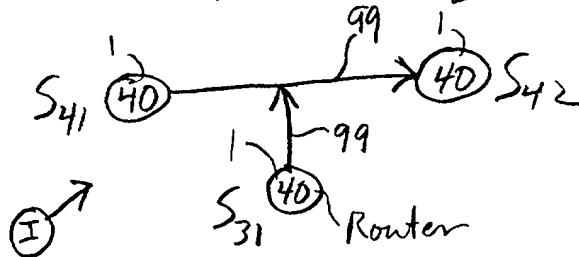


Fig. 16P



Figs. 16O-Q
are sections
of Fig. 16F
Net (left upper)

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like
Fig 10A
& 10B

Fig. 16X

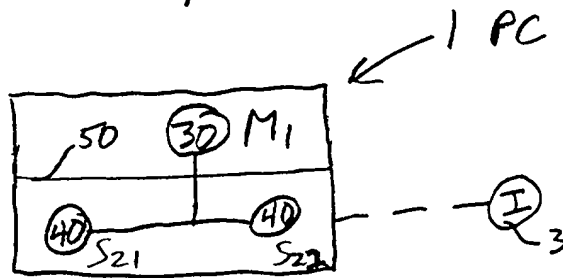


Fig. 16Y

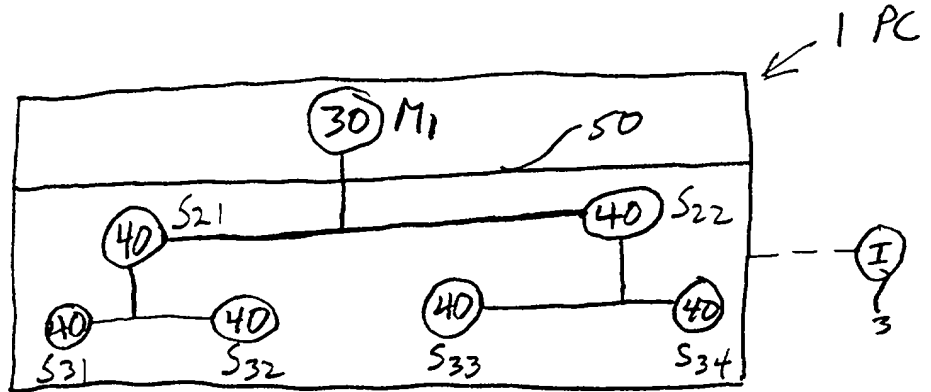


Fig. 16Z

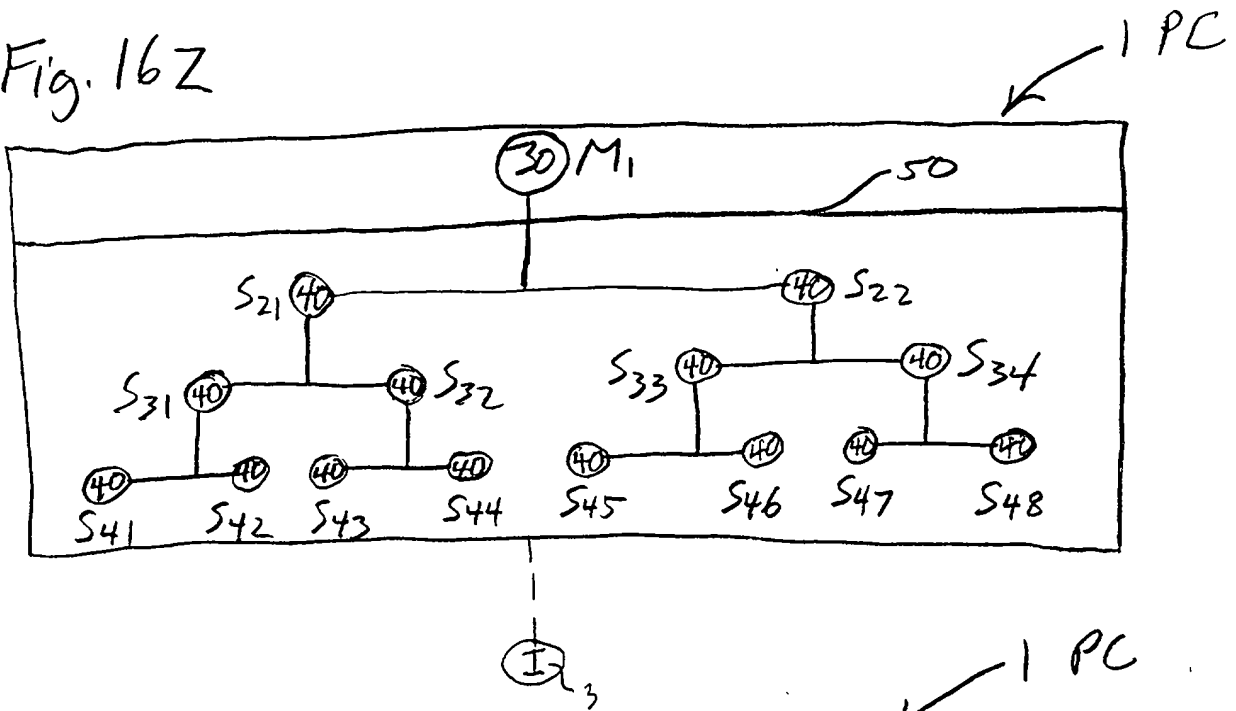


Fig. 16AA

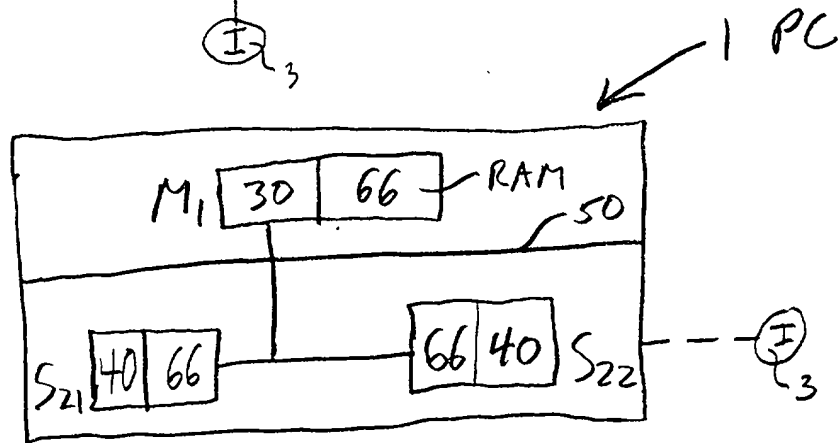
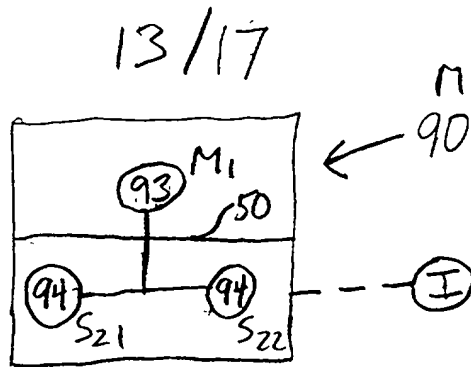


Fig. 16R



Like Fig. 10C:
"Personal Computer
on a chip"
(Figs. 16R-16U)

Fig. 16S

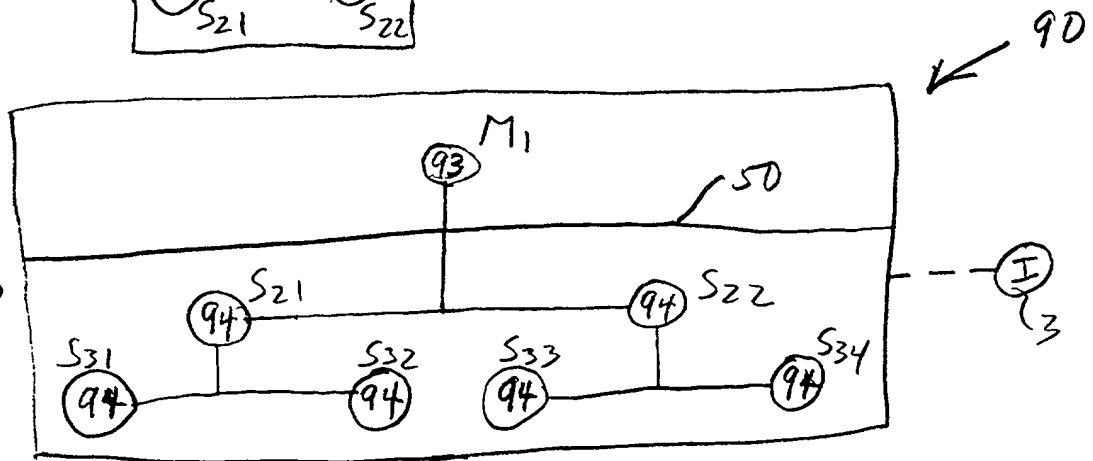


Fig. 16T

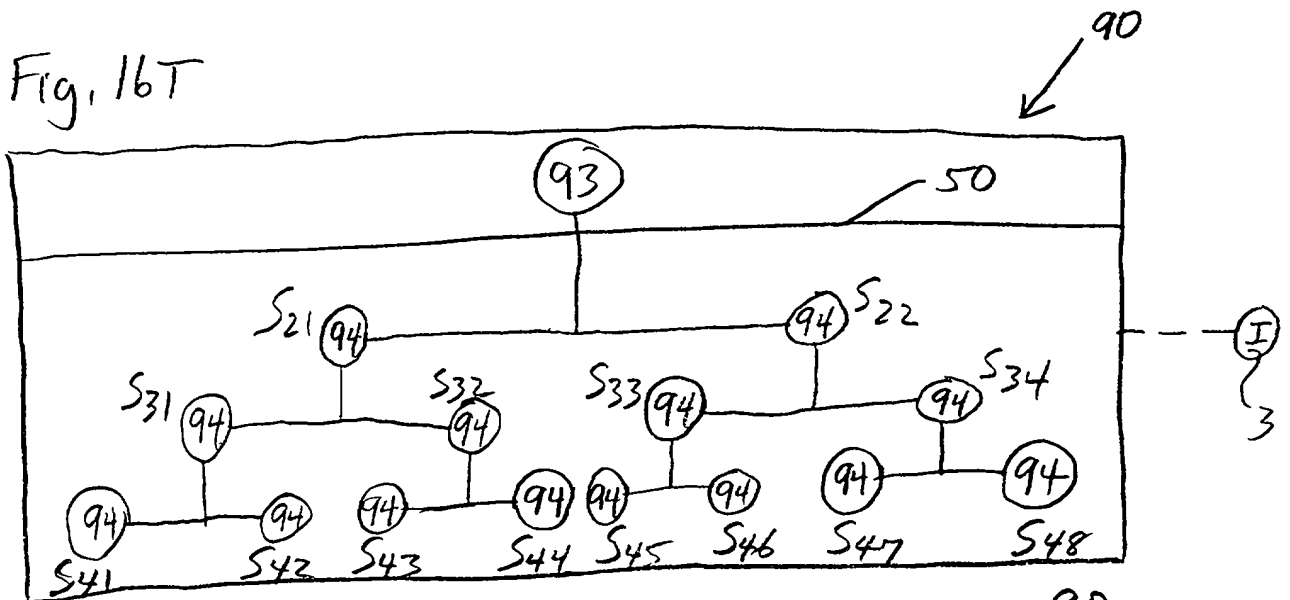
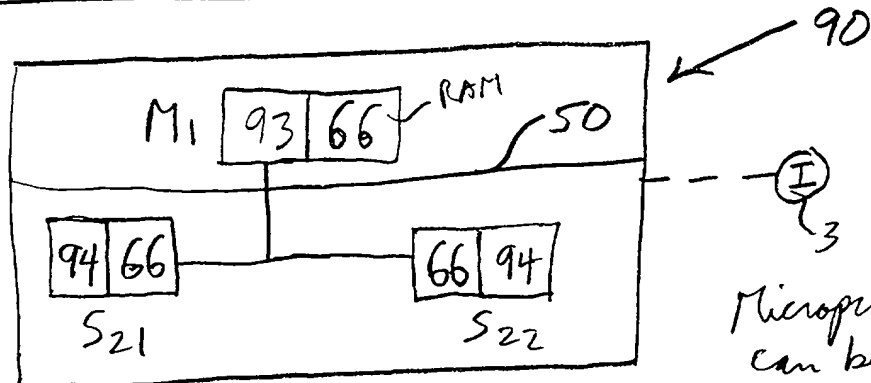


Fig. 16U



Microprocessor 90
can be entire
PC1. on a single
microchip

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Fig. 16V

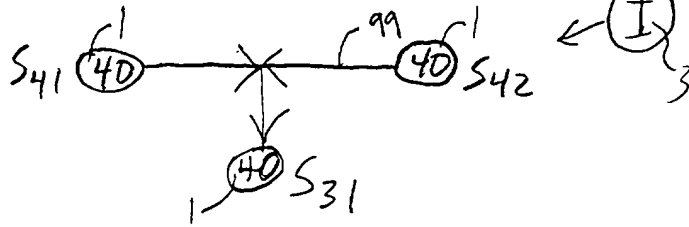


Fig. 16W-X
follows Fig.
16Q-Q &
are also sections
of Fig. 16F net

Fig. 16W

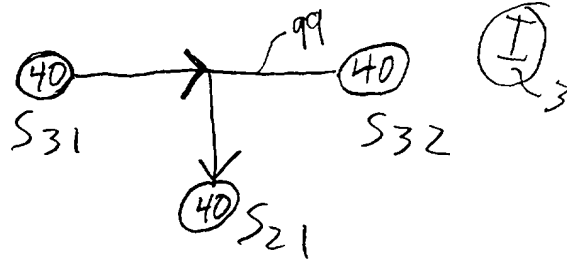


Fig. 17C

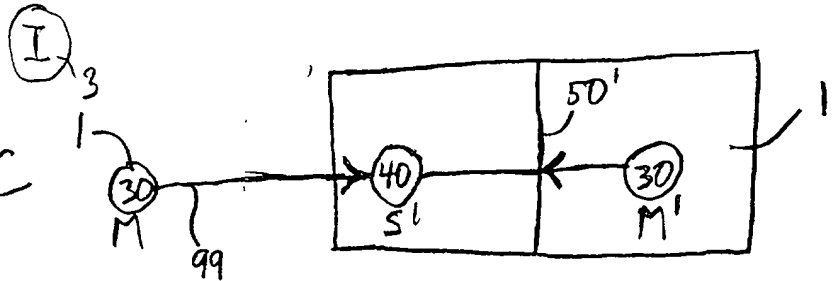


Fig. 17A

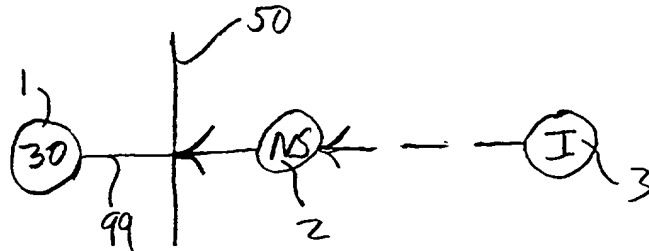


Fig. 17B

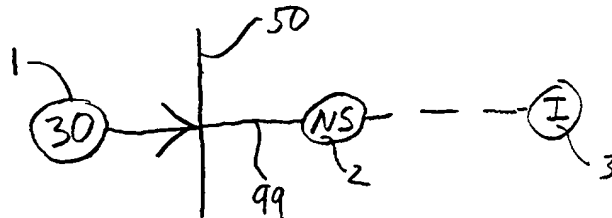
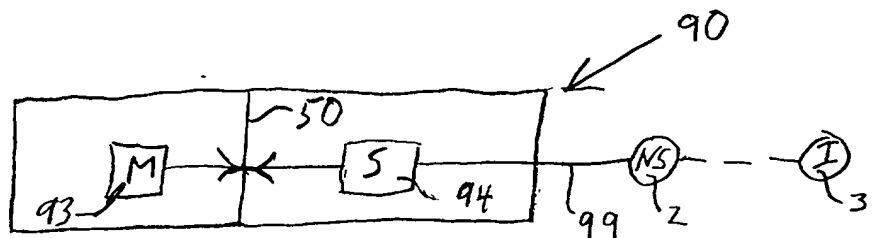


Fig. 17D



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Fig. 18A

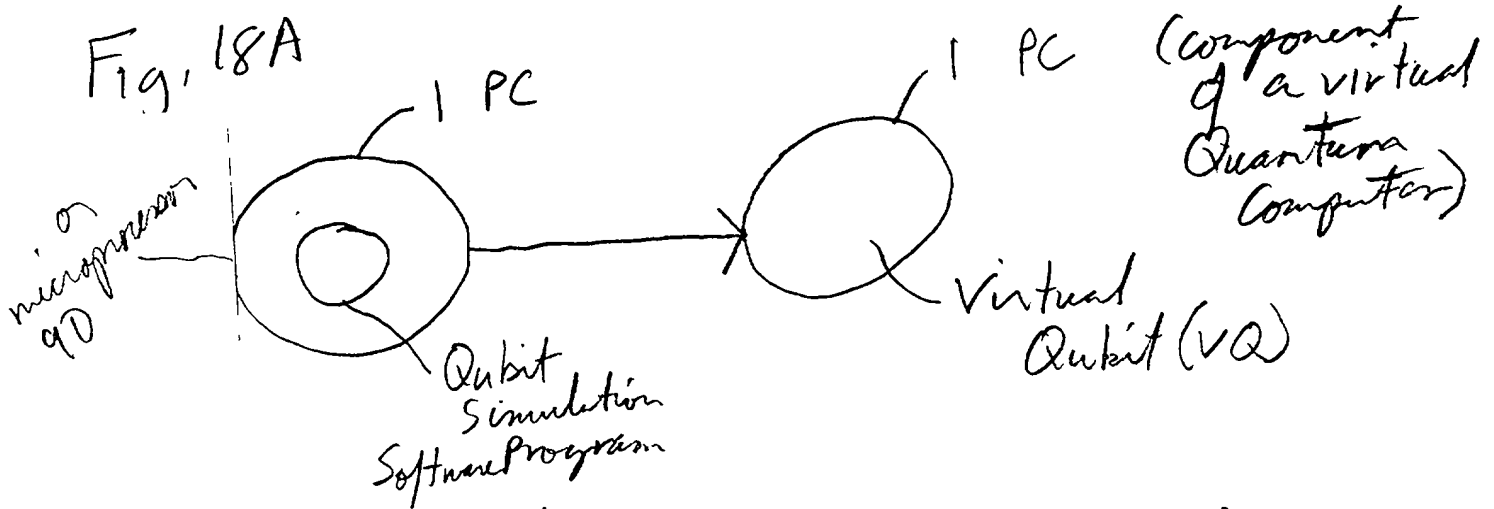


Fig. 18B

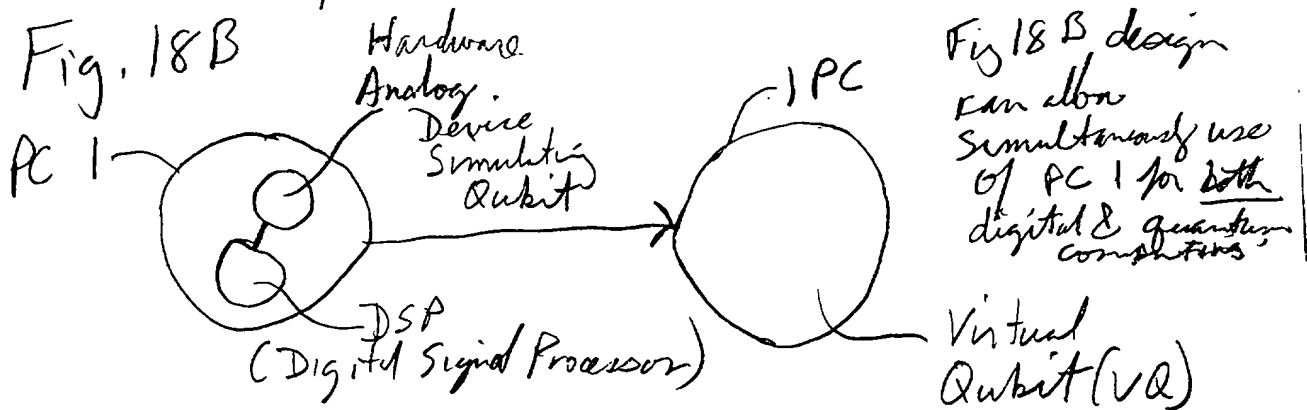


Fig 18 B design can also simultaneously use of PC 1 for both digital & quantum computers

Fig. 18C

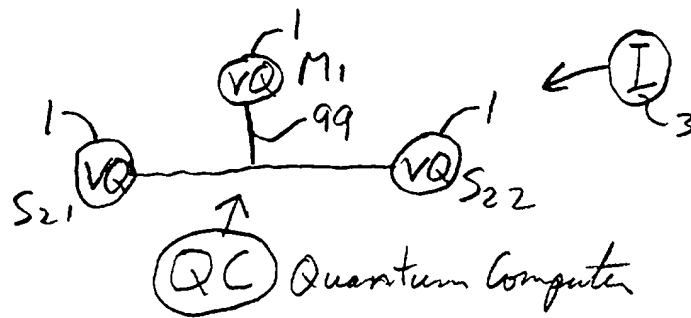
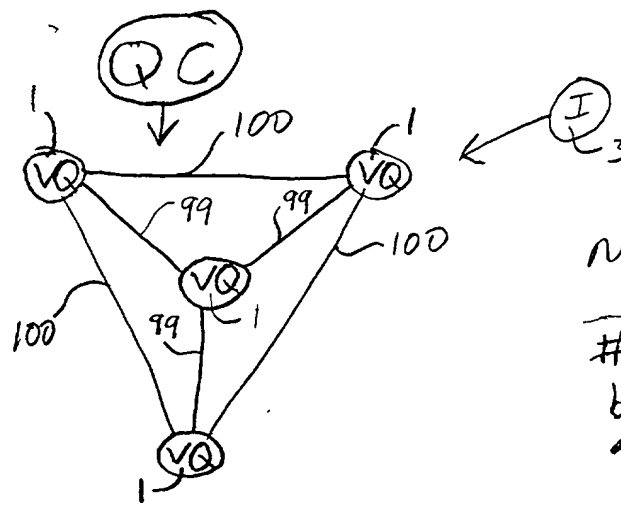


Fig. 18C like Fig. 16A & similarly VQ could be substituted for 30 & 40 in Figs. 16B-16Q & 16V-16AA and in earlier Figures

Fig. 18D

Like Fig. 13



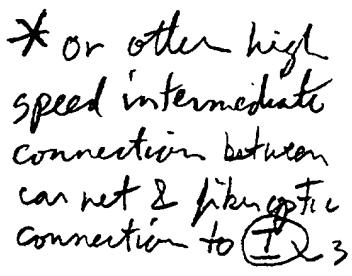
Note 99 & 100 mix

of VQ can be scaled to any size Quantum Computer QC

Connection device such as plug for external electrical power, recharge source and/or for optical fiber connection.*

Fig. 19

→
automobile
or other
transportation
vehicle



External
Focused (or focusable)
Light
Source
(to recharge
Solar Power cells)

Table 1. Demographic characteristics of the study population	
Age (years)	65.2 (SD 10.5)
Gender	
Male	55.2%
Female	44.8%
Education (years)	12.5 (SD 3.2)
Marital status	
Married	68.5%
Widowed	22.1%
Divorced	8.3%
Single	1.1%
Income (USD/month)	1,250 (SD 450)
Health status	
Good	72.3%
Fair	18.7%
Poor	9.0%

Fig. 20A

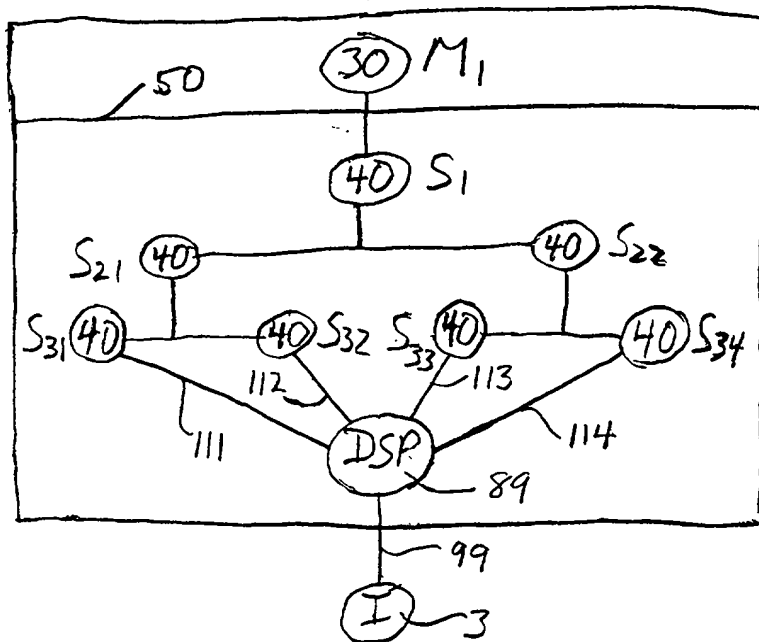
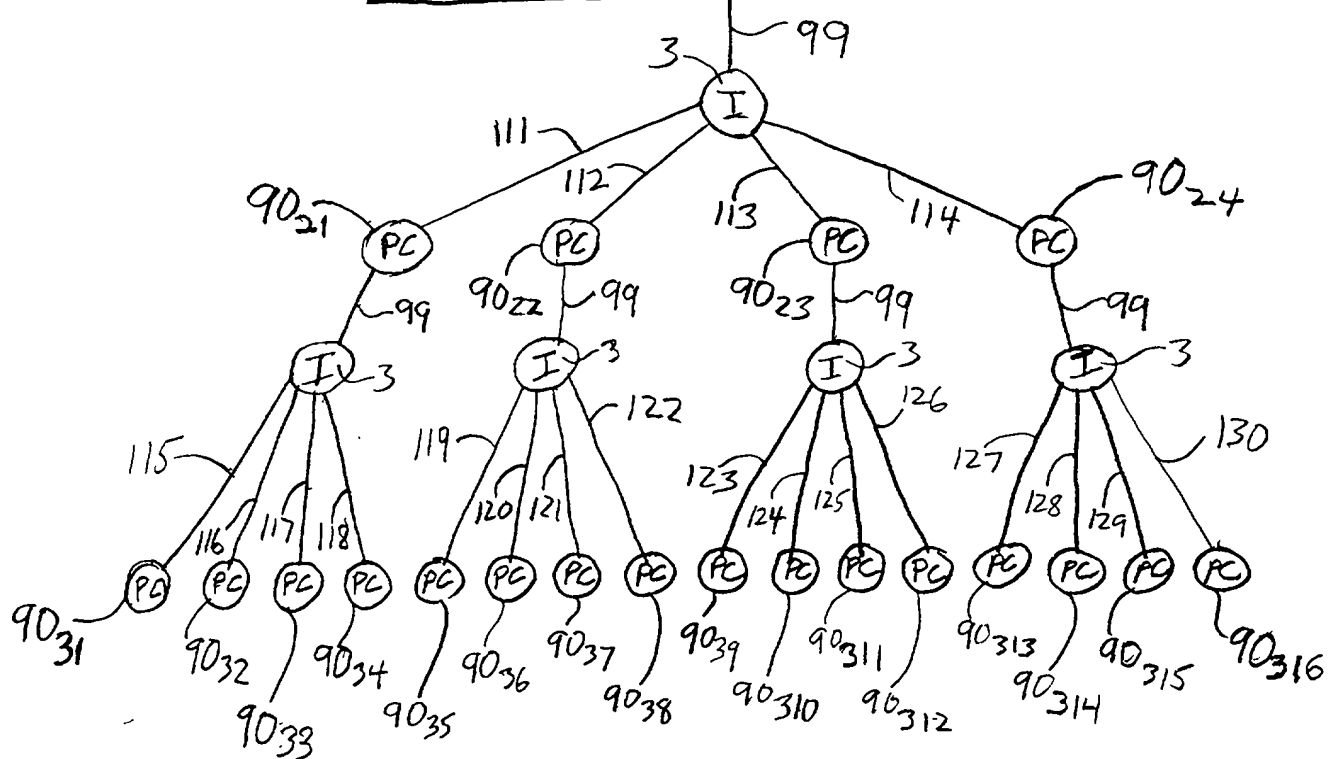
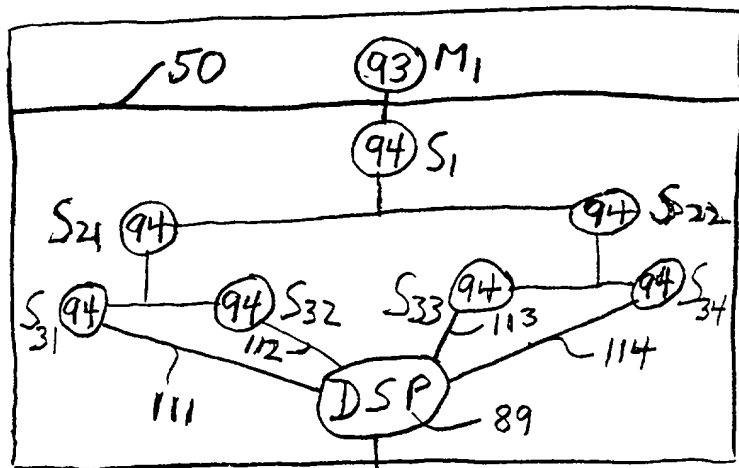


Fig. 20B



**VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS
(37 CFR 1.9(f) & 1.27(b))—INDEPENDENT INVENTOR**

Docket Number (Optional)

GNC 12 US

Applicant or Patentee: _____

Application or Patent No.: _____

Filed or Issued: _____

Title Global Network Computers

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees to the Patent and Trademark Office described in

☒ the specification filed herewith with title as listed above.

☐ the application identified above.

☐ the patent identified above.

I have not assigned, granted, conveyed, or licensed, and am under no obligation under contract or law to assign, grant, convey, or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e)

Each person, concern, or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below

☒ No such person, concern, or organization exists.

☐ Each such person, concern, or organization is listed below

Separate verified statements are required from each named person, concern, or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Frampton E. ELLIS, III

NAME OF INVENTOR

NAME OF INVENTOR

NAME OF INVENTOR

Signature of inventor

Signature of inventor

Signature of inventor

Date

Date

Date

Please type a plus sign (+) inside this box → ☒

PTO/SB/01 (3-97)
Approved for use through 8/30/98 OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION

☒ Declaration
Submitted
with Initial
Filing OR ☐ Declaration
Submitted after
Initial Filing

Attorney Docket Number	GNC12US
First Named Inventor	ELLIS, Frampton E
COMPLETE IF KNOWN	
Application Number	
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Global Network Computers

(Title of the invention)

the specification of which

☒ is attached hereto
OR

☐ was filed on (MM/DD/YYYY) as United States Application Number or PCT International

Application Number and was amended on (MM/DD/YYYY) (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, § 1.56

I hereby claim foreign priority benefits under Title 35, United States Code § 119 (a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365 (a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
PCT/US97/ 21812	PCT	11/28/97	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>	<input checked="" type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below

Application Number(s)	Filing Date (MM/DD/YYYY)	<input checked="" type="checkbox"/> Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto
60/033,871	12/20/96	
60/032,207	12/02/96	

[Page 1 of 2]

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Type a plus sign (+) inside this box → ☒

PTO/SB/04 (3-97)

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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I hereby claim the benefit under Title 35, United States Code §120 of any United States application(s), or §365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application

U.S. Parent Application Number	PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith ☐ Customer Number ☐ OR ☐ Registered practitioner(s) name/registration number listed below

Place Customer Number Bar Code Label here

Name	Registration Number	Name	Registration Number
N.A.			

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto

Direct all correspondence to: ☐ Customer Number or Bar Code Label ☐ OR ☒ Correspondence address below

Name	Frampton ELLIS				
Address	2895 S. Abingdon St., Suite B2				
City	Arlington	State	VA	ZIP	22206-1331
Country	USA	Telephone	703-951-6111	Fax	703-951-1116

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

Name of Sole or First Inventor:		<input type="checkbox"/> A petition has been filed for this unsigned inventor			
Given Name (first and middle (if any))			Family Name or Surname		
Frampton Erroll (III)			ELLIS		
Inventor's Signature					Date
Residence: City	Arlington	State	VA	Country	USA
Post Office Address	2895 S. Abingdon St.				
Post Office Address	Suite B2				
City	Arlington	State	VA	ZIP	22206-1331
				Country	USA

☐ Additional inventors are being named on the _____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

X

+

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DECLARATION — Supplemental Priority Data Sheet

Additional foreign applications:

[illegible]

Additional provisional applications

Application Number	Filing Date (MM/DD/YYYY)
60/031,855	11/29/96
60/066,313	11/21/97
60/066,415	11/24/97
60/068,366	12/19/97
(To be assigned)	5/22/97
(To be assigned)	5/22/97

Additional U S applications

U.S. Parent Application Number	PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number (if applicable)
08/980,058		11/26/97	

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